Spin Electronics

Interfacial Perpendicular Magnetic Anisotropy in Sub-20 nm Tunnel Junctions for Large-Capacity Spin-Transfer Torque Magnetic Random-Access Memory

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Abstract—Magnetic tunnel junctions (MTJs) with interfacial perpendicular magnetic anisotropy (PMA) attract much attention due to their utilization in spin-transfer torque magnetic random-access memory (STT-MRAM). Large interfacial PMA provides high thermal stability, which is critical for large-capacity MTJ arrays. We investigate the thermal stability and interfacial PMA needed for STT-MRAM applications. A thermal stability factor of 75 is required for data retention time of 10 years, which implies an interfacial PMA value of 4.7 mJ/m^2 as device sizes scale down to 10 nm. Even though a small retention time (e.g., 1 ms) is sufficient in some applications, such as cache memory, an interfacial PMA greater than 3.1 mJ/m^2 would be necessary for 10 nm MTJ pillars. When read disturbance is taken into consideration, the PMA should be larger. These findings provide guidelines for the design of sub-20 nm MTJ devices for large-capacity STT-MRAM.

Index Terms—Spin electronics, magnetic random-access memory, magnetic tunnel junction (MTJ), perpendicular magnetic anisotropy (PMA), spin electronics, thermal stability.

I. INTRODUCTION

Spin-transfer torque magnetic random-access memory (STT-MRAM) is widely considered as one of the promising candidates for the next-generation nonvolatile memory due to its fast speed, low power consumption, and unlimited endurance [Ikeda 2010, Hu 2011, Kent 2015]. In 2015, a 109 bit (1 Gbit) STT-MRAM with perpendicular magnetic anisotropy (PMA) was demonstrated [Park 2015]. The basic device is the CoFeB/MgO/CoFeB-based magnetic tunnel junction (MTJ), possessing a diameter of 40–50 nm, a tunnel magnetoresistance (TMR) ratio of 150%, and a switching current of 96 μA. Recently, Chung *et al.* [2016] presented a 4 Gbit STT-MRAM with 9 F^2 cell projection area, which is comparable to dynamic random-access memory (DRAM). Besides, Everspin Technologies announced fully functional 256 Mbit STT-MRAM product chips with the double data rate type three (DDR3) interface [Slaughter 2016]. These works have shown a bright future of large-capacity STT-MRAM applications.

One of those key challenges to further optimize memory density and switching current is achieving reliable data storage in small-node (e.g., 10 nm) MTJs for a long time [Amiri 2015, Kent 2015, Nowak 2016]. The industry standard requires 10 years retention time, which depends on the thermal stability of MTJs. However, in order to keep chip failure rate sufficiently low, higher thermal stability is needed for STT-MRAM with larger capacity. Moreover, for MTJs based on the interfacial PMA of the CoFeB/MgO/CoFeB structure (as shown in Fig. 1), the thermal stability decreases as the MTJ dimension scales down [Sato 2014]. Consequently, larger interfacial PMA is necessary for smaller MTJs. These problems have become the major obstacles for high-density STT-MRAM.

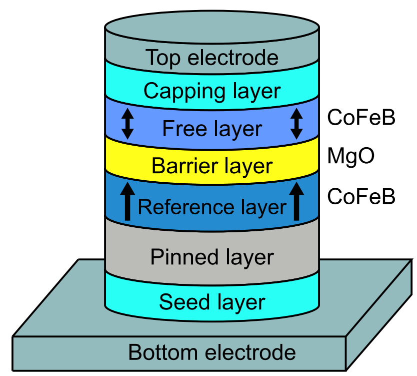

Fig. 1. Illustration of the MTJ stack based on the interfacial PMA of CoFeB/MgO/CoFeB structure.

In this letter, we provide a thorough investigation of the demand on thermal stability and interfacial PMA for STT-MRAM applications. The required thermal stability under different capacities are presented. Then, we discuss the interfacial PMA needed as a function of capacity and retention time. Finally, the impact of read disturbance is analyzed with scalability of MTJs taken into account.

II. THERMAL STABILITY ANALYSIS

The thermal stability of the free layer in an MTJ is characterized by the thermal stability factor Δ, which can be expressed as

$$\Delta = E_b/k_B T. \quad (1)$$

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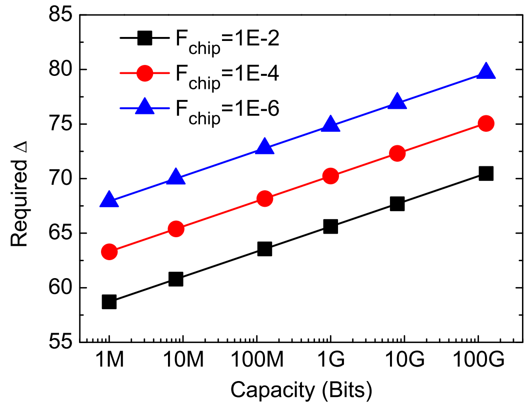

Fig. 2. Dependence of required thermal stability factor Δ on capacity with different chip failure rates F_{chip}. The points correspond to capacities of 1 Mbit, 8 Mbit, 128 Mbit, 1 Gbit, 8 Gbit, and 128 Gbit.

Here, E_b is the energy barrier between two stable states, k_B is the Boltzman constant, and T is the temperature. Due to thermal fluctuations, unintended switching of the magnetization in the free layer may occur. The switching probability of one MTJ after time t can be estimated using the following equation [Wernsdorfer 1997]:

$$P_{sw} = 1 - \exp\left[-\frac{t}{\tau_0}\exp(-\Delta)\right] \tag{2}$$

where the characteristic attempt time τ_0 is of the order of 1 ns. Furthermore, in a large MTJ array, all bits are required to maintain their states in the data retention period. Consequently, the chip failure rate for an STT-MRAM with N bits can be given as [Takemura 2010, Zhao 2012]

$$F_{\text{chip}} = 1 - \exp\left[-N\frac{t}{\tau_0}\exp(-\Delta)\right]. \tag{3}$$

Then, we can obtain the minimum thermal stability factor Δ to satisfy the required chip failure rate F_{chip} and retention time t

$$\Delta = -\ln\left[-\frac{\tau_0}{Nt}\ln\left(1 - F_{\text{chip}}\right)\right]. \tag{4}$$

Fig. 2 shows the dependence of the required thermal stability factor on capacity given a retention time of 10 years. It is clear that we need larger thermal stability to achieve lower chip failure rate. Moreover, the required Δ increases linearly with the $\ln(N)$. To be more accurate, an increase of 6.9 for Δ is necessary when the capacity is enlarged by 1000 times. Eventually, in order to achieve a capacity of 128 Gbit and a chip failure rate of 1E–4, the thermal stability factor should be larger than 75.

III. INTERFACIAL ANISOTROPY REQUIREMENT

MTJs with small lateral dimensions exhibit a single-domain behavior, where the spins in the free layer align along the same direction and switch together. The thermal stability factor can be expressed as

$$\Delta = \frac{KV}{k_B T} = \frac{K\pi D^2 t_{\text{CoFeB}}}{4k_B T}. \tag{5}$$

Here, K is the anisotropy energy density, V is the volume of the free layer, and D and t_{CoFeB} are the diameter and thickness, respectively. However, when D is larger than the nucleation size D_n, the nucleation-type reversal takes place, where the magnetization switching is induced by domain wall nucleation and propagation. In this case, the thermal stability factor was demonstrated to be independent [Sato 2011, 2012b, 2014] or linearly dependent [Chaves-O'Flynn 2015, Thomas 2015] on the MTJ diameter. The nucleation size D_n is of the order of the domain wall width δ_w, which can be approximately evaluated as $\delta_w = \pi\sqrt{A_s/K}$, where A_s is the exchange stiffness constant. For PMA-based CoFeB/MgO/CoFeB structures, the δ_w was reported to be from 30 to 140 nm [Sato 2012b, 2014, Piotrowski 2016]. In this letter, we focus on the small-node MTJs, especially MTJs with diameters smaller than 22 nm, and adopt the single-domain approximation in our calculations.

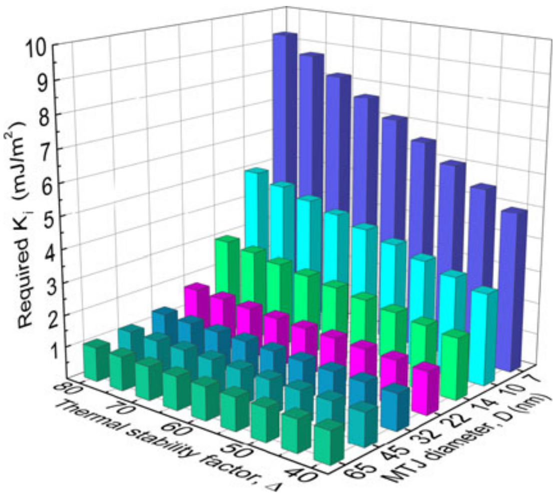

Fig. 3. Required interfacial anisotropy K_i as a function of thermal stability factor Δ and MTJ diameter D.

For an MTJ based on interfacial PMA of the CoFeB/MgO/CoFeB structure [Ikeda 2010, Yang 2011, Peng 2015], the anisotropy energy density K can be expressed as [Johnson 1999, Ikeda 2010]

$$K = K_b + K_i/t_{\text{CoFeB}} - 2\pi M_s^2(N_z - N_x) \tag{6}$$

where K_b is the bulk anisotropy, K_i is the interfacial anisotropy, M_s is the saturation magnetization, and N_z and N_x are the demagnetization factors along the perpendicular and in-plane directions, respectively. When the MTJ diameter is much larger than the free layer thickness, the $N_z - N_x$ is nearly constant 1. Nevertheless, as the device size becomes smaller, the $N_z - N_x$ decreases with the downscaling of the lateral dimension. In this case, the demagnetization factors can be approximately expressed as $N_z - N_x = 1 - 3\pi t_{\text{CoFeB}}/4D$, where D is the diameter of the MTJ [Mizunuma 2013, Sato 2014]. Previous studies demonstrated that bulk anisotropy K_b is negligible for the CoFeB/MgO/CoFeB-based MTJs [Ikeda 2010, Liu 2012, 2014, Lee 2014]. As a result, PMA originates mainly from K_i, which makes it essential to have large K_i so as to achieve enough thermal stability. By combining (5) and (6), we can get the relationship between the required K_i and the Δ

$$K_i \approx 2\pi M_s^2(N_z - N_x)t_{\text{CoFeB}} + \frac{4k_B T\Delta}{\pi D^2}. \tag{7}$$

Fig. 3 plots the required interfacial anisotropy under different thermal stability factors and MTJ diameters. Here, we assume the free layer thickness $t_{\text{CoFeB}} = 1$ nm, the temperature $T = 300$ K, and the saturation magnetization $M_s = 1250$ emu/cm^3 [Ikeda 2010, Liu 2012,

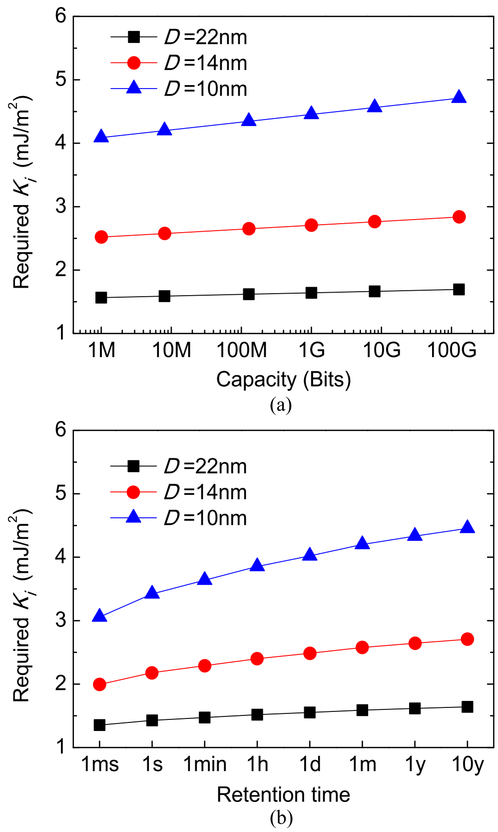

Fig. 4. Required interfacial anisotropy K_i as a function of (a) capacity and (b) retention time with different MTJ diameter D. (a) Retention time of 10 years is assumed. (b) Capacity of 1 Gbit is assumed.

Almasi 2015]. A linear dependence of the required K_i on the Δ can be observed from this figure. Moreover, the required K_i increases dramatically with downscaling of the MTJ size, especially when the device dimension is smaller than 32 nm. For MTJs with diameters from 32 to 65 nm, the typical K_i value of about 1.5 mJ/m^2 in the MgO/CoFeB/Ta structure is sufficient to achieve a thermal stability factor of 80. However, when the MTJ scales down to 14 nm and below, the interfacial PMA needs to be enhanced for applications with thermal stability requirement of $\Delta = 60$.

In the following, we analyze the relationship between the interfacial anisotropy and the capacity. By substituting (4) into (7), we can express the required K_i as

$$K_i \approx 2\pi M_s^2 (N_z - N_x) t_{\text{CoFeB}} - \frac{4k_B T}{\pi D^2} \ln\left[-\frac{\tau_0}{Nt}\ln\left(1 - F_{\text{chip}}\right)\right]. \quad (8)$$

Fig. 4 shows the calculation results of (8) with the chip failure rate of 1E–4. As we can see in Fig. 4(a), for MTJs with a dimension of 22 nm, the required K_i remains almost the same for different capacities. The K_i of 1.7 mJ/m^2 is needed for 128 Gbit STT-MRAM, which can be achieved with current technology [Worledge 2011, Gajek 2012, Liu 2012]. However, for MTJs with size of 10 nm, there is an obvious increase of the required K_i as the capacity increases. In this case, the K_i needed for 128 Gbit STT-MRAM reaches up to 4.7 mJ/m^2. Such a large interfacial PMA value has never been reported in experiments for the CoFeB/MgO/CoFeB-based structures. As a consequence, it remains a great challenge to scale down to small nodes (e.g., 10 nm) for large-capacity and nonvolatile STT-MRAM.

Nevertheless, for applications involving frequent read and write operations, such as the embedded cache and logic-in-memory architectures, a smaller retention time may be sufficient, which will lead to a relaxed demand on the interfacial anisotropy. Fig. 4(b) shows the required interfacial anisotropy as a function of the retention time. An obvious reduction of the required K_i can be observed as the retention time decreases from 10 years to 1 ms. However, even if a retention time of 1 ms is assumed, the K_i value of 3.1 mJ/m^2 is still needed for 10 nm MTJs. It is worth noting from Fig. 4(a) and (b) that MTJ size has the largest impact on the required interfacial anisotropy comparing with the capacity and retention time. Therefore, it is critical to attain large interfacial PMA in order to achieve small-node STT-MRAM.

IV. READ DISTURBANCE PROBLEM

In the above analysis, the retention mode is considered which assumes no read or write operations during the retention period. Actually, the read disturbance may also lead to unintended switching, which may further enlarge the demand on the thermal stability and the interfacial anisotropy. In particular, according to our previous work [Kang 2013, 2014, 2015], as the MTJ diameter scales down to a small node (e.g., <22 nm), the margin between the read and switching current decreases dramatically, leading to an enhancement of the required interfacial PMA. As a consequence, it is necessary to examine the effect of the read disturbance on the PMA requirement. The chip failure rate due to the read disturbance can be written as [Li 2004]

$$F_{\text{chip}} = 1 - \exp\left\{-m\frac{t}{\tau_0}\exp\left[-\Delta\left(1 - \frac{I_R}{I_{c0}}\right)\right]\right\} \quad (9)$$

where m is the number of bits per word, t is the cumulated read duration time, I_R and I_{c0} are the read current and the critical switching current, respectively. Accordingly, the required interfacial anisotropy can be expressed as

$$K_i \approx 2\pi M_s^2 (N_z - N_z) t_{\text{CoFeB}} - \frac{4k_B T}{\pi D^2}\frac{I_{c0}}{I_{c0} - I_R}\ln\left[-\frac{\tau_0}{mt}\ln\left(1 - F_{\text{chip}}\right)\right]. \quad (10)$$

Fig. 5 shows the required interfacial anisotropy K_i as a function of read/switching current ratio I_R/I_{c0} assuming 32 bits per word. The corresponding I_{c0} values are shown along the top abscissa axis with the assumption of $I_R = 10\ \mu$A. Larger interfacial PMA is necessary for longer read duration and lower chip failure rate. Moreover, the required K_i is further enhanced with the increase of I_R/I_{c0}. When the MTJ size shrinks down, the I_{c0} scales quadratically with the MTJ diameter, leading to an enlargement of the I_R/I_{c0} [Gajek 2012, Kang 2015]. As indicated by the dashed line in Fig. 5, when the I_R/I_{c0} is larger than 30%, corresponding to I_{c0} smaller than 33 μA under $I_R = 10\ \mu$A, a stronger requirement on the K_i comes from the read disturbance rather than the thermal fluctuations. Consequently, the required interfacial PMA is further enlarged when the read disturbance is taken into account.

Several methods can be used to enhance the interfacial PMA in the CoFeB/MgO/CoFeB-based MTJs. One of them is to use a double-interface structure which employs the MgO/CoFeB/Ta/CoFeB/MgO stack as the recording layer [Sato 2012a, 2013]. By introducing two CoFeB/MgO interfaces in this structure, the thermal stability can be increased by a factor of 1.9. However, when the MTJ size scales down

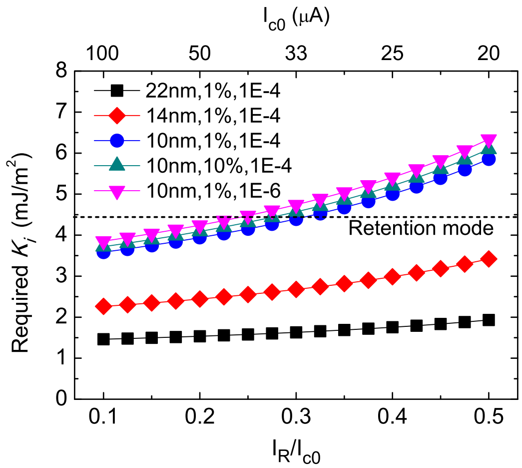

Fig. 5. Dependence of required interfacial anisotropy K_i on read/switching current ratio I_R/I_{c0} with MTJ sizes of 22, 14, and 10 nm, cumulated read durations of $1\% \times 10$ years and $10\% \times 10$ years, and chip failure rates of 1E–4 and 1E–6. The top abscissa axis shows the corresponding switching current I_{c0} with the assumption of read current $I_R = 10\ \mu A$. The dashed line indicates the required K_i in a retention mode with 10 nm diameter, 10 years retention time, 1 Gbit capacity, and chip failure rate of 1E–4.

to 20 nm, the thermal stability factor in this structure was lower than 50, which could not meet the demand of large-capacity STT-MRAM [Sato 2014]. Another method is to utilize proper capping and seed materials. Several experimental works reported that the capping and seed layers were also very important to the PMA. For example, in-plane anisotropy was observed with a Ru seed layer, whereas the PMA was achieved with the Ta seed layer [Worledge 2011]. Moreover, some other materials such as Hf, Mo, W, and Nb were found to induce larger PMA than Ta [Liu 2012, 2014, Lee 2014, An 2015]. These variations of PMA are attributed to the different interfacial anisotropy at the CoFe/heavy metal interface [Peng 2015]. Furthermore, it is predicted that the MgO/CoFe/Bi structure gives rise to giant interfacial PMA (6.09 mJ/m^2) [Peng 2017], which is about three time larger than that of the MgO/CoFe/Ta structure, making it promising to achieve large-capacity and small-node STT-MRAM with sufficient thermal stability.

V. CONCLUSION

In summary, we provide a comprehensive investigation of the required thermal stability and interfacial PMA of MTJs for STT-MRAM applications. In order to achieve large-capacity STT-MRAM, high thermal stability is needed, leading to a strong requirement on the interfacial PMA. It is found that MTJ size has the largest impact on the required interfacial anisotropy comparing with the capacity and retention time. Moreover, for 128 Gbit memory with a retention time of 10 years and the MTJ size of 10 nm, the thermal stability factor of 75 and the interfacial anisotropy of 4.7 mJ/m^2 are required. Moreover, frequent read operations with large read/switching current ratio may further enlarge the demand on PMA. The double-interface structure can be used to enhance interfacial anisotropy. However, improvement in material engineering is still necessary when MTJ sizes scale below 20 nm.

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