Cr metal thin film memory

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As state of the art flash memory technologies scale down to sub 30 nm node, conventional floating gate flash memory approaches its physical scaling limit mainly because of the high gate coupling ratio (GCR) requirement to secure proper memory window. Here, we report a novel flash memory device called Cr metal thin film memory (MTFM) that can circumvent the GCR issue and extend flash memory scalability by employing Cr thin film as a storage layer. Cr metal thin film memory devices with simple and low temperature processes produced a wide memory window of 10 V at the ±18 V voltage sweep with GCR of only 0.3. Such a large window can be adopted for multi-level cell operations, which can further increase the memory density. Also, retention measurement shows more than 10 years retention time due to higher energy barrier between Cr metal and tunnel oxide than conventional poly silicon and tunnel oxide. Cross section transmission electron microscope (TEM) images showed the structure and accurate dimensions of the Cr MTFM device with continuous Cr film and sharp interfaces. As for material characterizations, an amorphous like Cr phase was observed through TEM and x-ray diffraction (XRD). X-ray photoelectron spectroscopy (XPS) confirmed the Cr-Cr bond and Cr-O bond near the Cr surface after evaporation and rapid thermal annealing. This metal thin film memory may open a new route to achieve the terabit level flash memory. © *2011 American Institute of Physics*. [doi:10.1063/1.3626901]

I. INTRODUCTION

The gate coupling ratio (GCR) is the ratio of control oxide capacitance to total gate capacitance that determines the actual voltage applied to the tunneling oxide in flash memory devices. This GCR is one of the most important figures of merit in flash memory devices, which secures the required memory window at a given gate voltage. However, the high GCR (> 0.5) requirement in state of the art flash technologies limit the flash memory scalability because of control oxides surrounding poly-Si floating gate.[1]

One straightforward solution to resolve this scalability issue from the GCR requirement is to develop a planar type flash memory that shows wide enough memory window. A planar type flash memory called charge trap flash (CTF) memory which uses thin silicon nitride film as a charge storage layer was suggested as a replacement to the floating gate (FG) flash memory because of its higher scalability and lower power consumption.[2] However, defect-assisted data storage in CTF memory devices may result in erasing saturation and thermal instability issues.[3] Also, it is difficult to control the amount of defect sites precisely, which can cause variability issue in terms of the memory window.

A promising candidate to solve this defect-assisted data storage and produce a wide memory window for larger memory density is to employ a metal thin film as a storage layer. Because metal inherently has a high density of states at the Fermi level, more electrons can be stored in these states than those stored in defect states.[4] Also, this high density of states of metal layer alleviates the Coulomb blockade effect as the device size shrinks, which results in longer retention time in memory devices compared to memories with semiconductor nanocrystals.[5]

In this study, we report the first demonstration of the metal thin film memory in which Cr metal thin film deposited by a simple e-beam evaporation method was used as a charge storage layer. Transmission electron microscopy (TEM) study showed unique features of the resulting memory device and enabled feature sizes that are critical to evaluate device performance. Cross section transmission electron microscope (TEM) images showed continuous Cr film and sharp interfaces of the fabricated device. An amorphous like Cr phase was observed through TEM and x-ray diffraction

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(XRD). X ray photoelectron spectroscopy (XPS) confirmed the Cr-Cr bond and Cr-O bond near the Cr surface after evaporation and rapid thermal annealing. The fabricated metal thin film memory device showed an excellent memory effect of a 10 V memory window at the $\pm$18 V program/erase voltages.

II. EXPERIMENTAL

A schematic process flow of the proposed fabrication method is shown in Fig. 1. A 4 in low doped Si wafer (bboron doped, 10^{15} cm^{-3}) was cleaned by Piranha ($H_2SO_4 + H_2O_2$) and dipped into a buffered oxide etchant (BOE, $HF + NH_4F + H_2O$) to remove any residual native oxide. Then 5 nm tunnel oxide was grown by a rapid thermal oxidation (RTO) system. Tunnel oxide thickness was measured after RTO by an ellipsometer (SOPRA). A layer of 15 nm thick chromium (Cr) was deposited by e-beam evaporation (Fig. 1(c)). As for the e-beam evaporation conditions, the source to substrate distance was 18 in, the angle of incidence between the ion beam and the plane of the substrate was 5° and the vacuum level was 5×10^{-6} Torr. The evaporation rate was 1.0 A/sec. A 30 nm Al_2O_3 was deposited as a control oxide (Fig. 1(f)) by an atomic layer deposition (ALD, Cambridge Nanotech) and the 10 nm/800 nm Ti/Al layers were deposited by an e-beam evaporator (CHA30) through a shadow mask with a hole area of $7 \times 10^{-4}cm^2$. Then, each device was isolated by chlorine (Cl_2) dry etch (Unaxis SLR770 ICP Minispec) using metal electrode as a etch mask.

About 300 nm thickness metal electrode remained after 45 s Cl_2 etch. Remaining metal height was measured by a surface profiler (Dektak 6M). A capacitive structure of the metal thin film memory device was completed for electrical testing (Fig. 1(f)) after depositing 200 nm Al back contact to lower the substrate resistance. Post annealing was done at 450 °C for 30 s by rapid thermal process (RTP) in N_2 ambient.

III. RESULTS AND DISCUSSION

To determine the detailed structural characteristics of the metal thin film memory, cross sectional transmission electron micrographs (TEM, FEI Tecnai F20) were obtained. TEM images are shown in Fig. 2. Figure 2(a) shows the bright-field TEM image of a fabricated memory device. The actual Cr metal layer thickness is 17 ($\pm$0.5) nm which is about 2 nm thicker than the programmed thickness on e-beam evaporator. The control oxide thickness (Al_2O_3) is determined to be 30 nm which coincides with the expected value from ALD (300 cycles, 1 A/cycle). Quality and thickness of the control oxide is critical because electron transfer from the top electrode to Cr metal layer has to be minimized to maximize the memory effect.[6] The high resolution TEM (HRTEM) investigations (an example is shown in Fig. 2(b)) revealed that tunneling oxide thickness is measured to be 5($\pm$0.5) nm. Accurate tunnel oxide thickness is critical for evaluating device performance because tunneling efficiency depends heavily on tunneling barrier width.[4] No apparent crystalline phases in Cr thin film were observed throughout the HRTEM images. Moreover, by tilting the Cr to directions other than the Si zone axis (Fig. 2(b)), no fringes or lattices were observed for the Cr thin film in the HRTEM images, which indicates that the Cr thin film mostly consists of amorphous phases. This amorphous phase was possibly formed because the Cr deposition was carried out at room temperature so there was insufficient energy for diffusion to form a crystalline structure. However, existence of Cr polycrystalline phases cannot be excluded completely. In terms of the memory device performance, differences between polycrystalline Cr thin film and amorphous Cr thin film has not been studied yet.

To further characterize the Cr thin film which was used as a charge storage layer in the memory device, x-ray diffraction (XRD) and x-ray photoelectron spectroscopy (XPS) were taken. Figure 3 shows x-ray diffraction patterns of as deposited Cr thin film (Fig. 3(a)) and annealed Cr thin film (Fig. 3(b)) at 450 °C for 30 s by a rapid thermal process (RTP). Peaks with relatively strong intensity correspond to Si crystalline peaks and no apparent peak for Cr crystalline[7] was observed. XRD pattern of the annealed sample shows no major difference with as deposited sample, as can be seen from Fig. 3(b). XRD was taken on four different samples with and without annealing on eight different spots, and no Cr peak was observed with the maximum process temperature (450 °C) used for this study. These results support the observations from HRTEM images that showed the amorphous like phase of Cr thin film.

Because no clear evidence could be provided on the existence of Cr phase by TEM and XRD study, x-ray photoelectron spectrum (XPS, Omicron ultra high vacuum XPS/UPS system) was taken on Cr thin film. For the x-ray source, Al Kα X-ray was used with a take-off angle of 90°. Figure 4(a) shows the Cr $2p_{3/2}$ peak at 574.4 eV and Cr $2p_{1/2}$ peak at 583.6 eV. Also, the Cr_2O_3 $2p_{3/2}$ peak at 576.7 eV and Cr_2O_3 $2p_{1/2}$ peak at 586.1 eV are observed. These peak values correspond with the work by Salvi *et al.*[8] Fig. 4(b) shows the O 1s spectrum of Cr_2O_3. O 1s shows a broad peak because two oxygen peaks are overlapped. These two peaks around 530 eV and 531 eV are due to substitutional oxygen, as well as those oxygen species associated with interstitial and surface sites.[9] Therefore, XPS study confirmed the

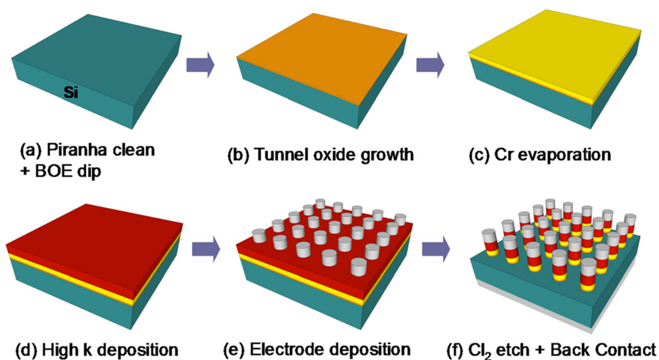

FIG. 1. (Color online) Schematic process flow of the proposed metal thin film memory in capacitive structure: (a) Piranha clean and BOE dip, (b) 5 nm thermal oxide growth by rapid thermal oxidation (RTO), (c) 15 nm Cr deposition by e-beam evaporation, (d) High K dielectric deposition by atomic layer deposition (ALD), (e) metal gate deposition by e-beam evaporation, and (f) device isolation by Cl_2 etch and making back contact to lower substrate resistance.

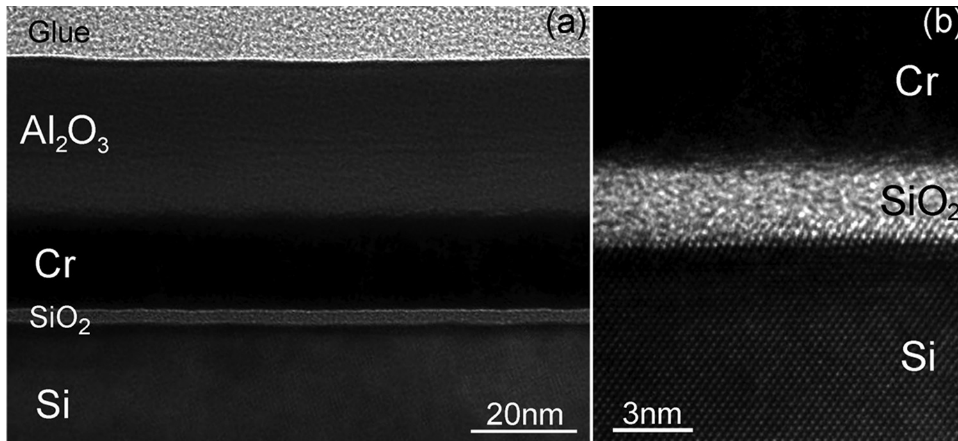

FIG. 2. Cross sectional HRTEM images of the fabricated memory device. (a) Low magnification TEM image shows Cr thickness of 17 (±0.5) nm and 30 nm Al_2O_3. (b) High resolution TEM image shows 5 (±0.5) nm tunnel oxide thickness and no apparent crystalline phases in Cr.

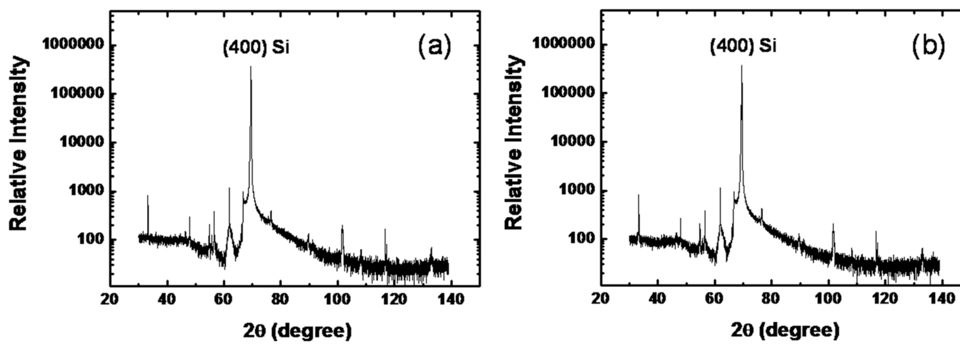

FIG. 3. X ray diffraction patterns of (a) as deposited Cr thin film and (b) annealed Cr thin film on single crystal (100) Si substrate with 5 nm SiO_2. XRD patterns show no evidence of Cr crystalline peak.

existence of the Cr-Cr bond and revealed that Cr_2O_3 was formed near the surface after e-beam evaporation, which is well known for Cr materials.

Capacitance-voltage curves of the fabricated devices at 100 kHz with and without Cr metal thin film are plotted in Fig. 5(a) and Fig. 5(b). The control sample without Cr metal thin film was fabricated by Piranha cleaning, BOE dip, 5 nm RTO and 30 nm Al_2O_3 ALD in sequence. Calculated GCR for the memory device from Eq. (1) is only 0.3, which is far less than the industrial requirement, where C_{con} is the control oxide capacitance and C_{tun} is the tunnel oxide capacitance. Because the proposed device is a planar type device, GCR can be derived from thickness and relative dielectric permittivity of both control oxide and tunnel oxide. Therefore, 30 nm thick Al_2O_3 ($\epsilon_r = 10$) and 5 nm thick SiO_2 ($\epsilon_r = 3.9$) obtained from HRTEM images result in GCR of 0.3.

$$GCR = \frac{C_{con}}{C_{tun} + C_{con}} \tag{1}$$

However, a counterclockwise hysteresis loop in Fig. 5(a) obtained by forward and backward bias sweeps from −18 V to 18 V shows an excellent memory effect of the device with Cr metal thin film. A threshold voltage shift (ΔV_{th}) of 10 V is seen in Fig. 5(a). This wide memory window with such a low GCR is considered to be due to the high Cr density of states at the Fermi level. From a handbook,[10] chromium density of states at its Fermi level is known to be 1.4×10^{22} cm^{-3} whereas Si effective density of states in the conduction band is 2.8×10^{19} cm^{-3}.[11] This high density of states of Cr allows planar type flash memory device with a large window, which can achieve higher memory density beyond state of the art floating gate flash memory devices. Ten cycles of

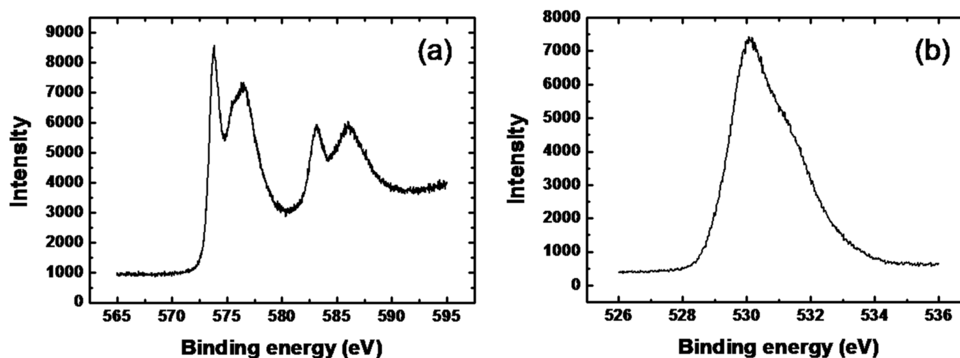

FIG. 4. X-ray photoelectron spectroscopy (XPS) of Cr thin film deposited by e-beam evaporation. (a) Cr 2p spectrum and (b) O 1s spectrum indicate the existence of Cr_2O_3 as well as Cr near the surface

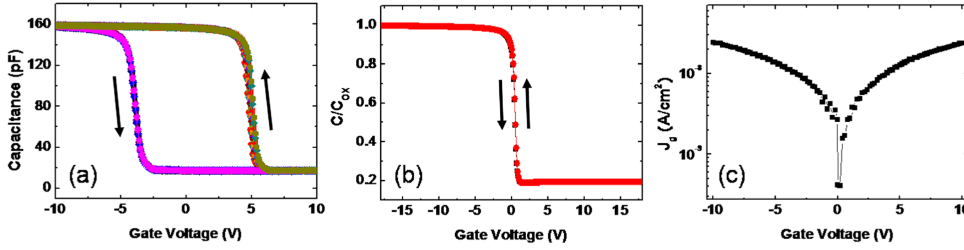

FIG. 5. (Color online) (a) Capacitance-voltage (C-V) curve of the proposed memory device showing memory function with an ultra-wide memory window of 10 V at ± 18 V voltage sweep. (b) C-V curve of the control sample without metal thin film showing no hysteresis with steep transitions. (c) Memory device showing low leakage current density.

forward and backward bias sweeps show precise memory window of 10 V at ±18 V bias sweep condition. Because the minimum memory window required for flash memory is 1.5 V,[12] a 10 V window suggests that Cr metal thin film memory device can be used for multi-level cell memory application that may have up to 3 bits per cell. Apparently, the memory window of Cr metal thin film at a given gate voltage is smaller than Cr metal nanodot memory reported[13] because of smaller GCR in Cr metal thin film device. The total oxide capacitance of the memory device at the accumulation region was 160 pF and therefore, the equivalent oxide thickness (EOT) was calculated to be 15 nm using $t_{OX} = \frac{\varepsilon_{OX}}{C_{OX}} \times A$, where $\varepsilon_{OX} = 3.45 \times 10^{-13}$ F/cm for SiO_2 and area $A = 7 \times 10^{-4}$ cm^2. Flat capacitance values at the accumulation region (160 pF) and inversion region (21 pF) throughout the bias sweep range (±18 V) (Fig. 5(a)) imply the excellent quality of ALD Al_2O_3 film covering Cr metal film because a leaky control oxide would increase accumulation capacitance, as additional charges could be induced to the oxide, meanwhile capacitance would decrease as the charges were extracted from the oxide at the inversion region. Steep transitions without any kinks from accumulation to inversion and vice versa imply the low interface states at the SiO_2/Si interface,[13] which proves the effectiveness of the cleaning process (Piranha and BOE) and the following rapid thermal oxidation. The control sample without metal thin film also showed the flat capacitance values at both accumulation and inversion regions with steep transitions (Fig. 5(b)) More important, the control sample showed no apparent hysteresis loop with a ±18 V bias sweep. This is strong evidence that the programmed charges in the metal thin film memory device were mostly stored at the metal film, not in the oxide or at the interfaces. These low leakage current and low interface states are critical for the high performance of the device such as large memory window, long retention time, and high reliability.[14] Threshold voltage shift of the metal thin film memory device can be described as Eq. (2), because higher gate voltage is needed to compensate stored charges on Cr film underneath the control oxide, which results in the shift of V_{th},

$$\Delta V_{th} = \frac{Q}{\varepsilon_{con}} \times t_{con} \tag{2}$$

where Q is the stored charge density (C/cm^2) in the metal film, t_{con} is the control oxide thickness, and ε_{con} is permittivity of the control oxide. Substituting $\Delta V_{th} = 10$V, $\varepsilon_{con} = 8.85 \times 10^{-13}$F/cm, and $t_{con} = 3 \times 10^{-6}$cm, Q is calculated to be 2.95×10^{-6}C/cm^2. Using the device area (7×10^{-4}cm^2), average 2.06×10^{-9}C is stored in the device. Therefore, one device stores up to about 1.3×10^{10} electrons during the program, as one electron has the charge of 1.6×10^{-19} C. It is observed that the device can be completely erased and even over erased to below 0 V threshold voltage. This is because the Al_2O_3 control oxide had a low leakage current so that the electrons injected from the gate metal to Cr metal film were effectively blocked during erase operation while electrons could be injected from the Cr metal film to the Si substrate through the tunneling oxide, which resulted in the over erase. The large over erase in Fig. 5(a) (> −2 V) is beneficial because it reduces the overall program/erase voltage for multi level cell operation. Figure 5(c) shows a dc leakage current density (A/cm^2) through the device. Low leakage current densities, less than 5×10^{-8}A/cm^2, were achieved at ±10 V, which were expected from the flat C-V curves and TEM images. Figure 6(a) shows retention characteristics of the Cr metal thin film memory. Retention measurement at room temperature shows a 13% charge loss at 10 years of retention time with 5 nm thick tunnel oxide. Fig. 6(b) shows three possible mechanisms for charge loss during retention—Schottky emission (SE), Fowler-Nordheim tunneling (FNT), and direct tunneling (DT). These three mechanisms depend exponentially on the barrier height between Cr work function and dielectric work function (Φ_B).

The next figure of merit for flash memory devices is retention time, which refers to the potential lifetime of non-volatile storage. Generally, retention time requirements are more than 10 years before the device loses 50% of stored charge. Loss of storage is typically the result of charge tunneling from the floating gate through the tunnel oxide. Three possible charge loss mechanisms during retention are Schottky emission (SE), Fowler-Nordheim tunneling (FNT), and direct tunneling (DT). We note that these three mechanisms depend exponentially on the barrier height between Cr work function and dielectric work function (Φ_B). In traditional polysilicon/SiO_2 devices, the barrier height is fixed and is simply the difference between the SiO_2 conduction band edge (0.95 eV) and that of polysilicon (4.02 eV). This means that the minimum tunnel oxide thickness is limited to 7–8 nm to guarantee 10 year retention time. By contrast, the Cr/SiO_2 system offers a larger electronic barrier height due to the higher work function of chromium (4.55 eV). This allows for the tunnel oxide to be further thinned.

The final figure of merit that should be discussed in flash memory is reliability. In general, reliability largely depends

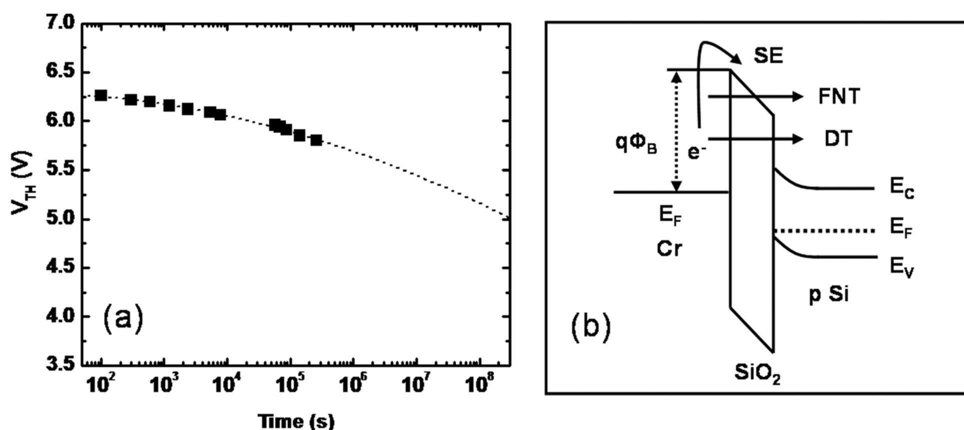

FIG. 6. Band structure of our Cr/SiO_2 junction and experimental data for retention time with a tunnel oxide of 5 nm. Measurements indicate a charge loss of 13% after 10 years, more than adequate for practical devices.

on oxide quality or thickness because the number of program/erase cycles can permanently damage oxide, thus resulting in charge loss. However, metal storage elements can have more serious issues of metal diffusion into the tunnel oxide or metal reaction with the tunnel oxide. This is indeed a serious concern with metal nanocrystal memories because most of metal nanocrystal memories previously reported were using high temperature rapid thermal processes to form nanocrystals.[4] Cr metal film memory has many fewer diffusion or reaction problems because Cr film was deposited at room temperature using an e-beam evaporator. The high temperature process of source/drain dopant activation could also affect reliability of Cr metal thin film memory, which is not studied here. However, NAND flash without source/drain implantation is reported to be more immune to short channel effect.[15] Therefore, Cr metal film memory will not have more reliability issues than conventional floating gate flash memory devices as the maximum process temperature can be claimed as low as 450 °C after tunnel oxide growth.

IV. CONCLUSION

In summary, a novel Cr metal thin film memory device has been proposed and demonstrated. Due to higher Cr density of states than silicon, which is used in conventional flash memory device, a wide memory window of 10 V was achieved at ±18 V voltage sweep despite oflow gate coupling ratio. Because Cr metal thin film device is a planar type device, scaling down beyond the physical scaling limit of floating gate flash memory device is possible. This wide memory window can also be adopted for multi-level cell applications, which can further increase the memory density. Also, retention characteristics showed more than 10 years of retention time with relatively thinner tunnel oxide because of higher barrier height provided by Cr. Therefore, a metal thin film memory with a simple and reliable process may open new opportunities for terabit memory applications.

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