Diode-MTJ Crossbar Memory Cell Using Voltage-Induced Unipolar Switching for High-Density MRAM

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***Abstract*— This letter presents a diode-magnetic tunnel junction (MTJ) magnetic random access memory cell in a 65-nm complimentary metal-oxide-semiconductor compatible process. A voltage-controlled magnetic anisotropy switching mechanism, in addition to STT, allows for a unipolar set/reset write scheme, where voltage pulses of the same polarity, but different amplitudes, are used to switch the MTJs. A small crossbar array is constructed from 65-nm MTJs fabricated on a silicon wafer, with switching voltages ∼1 V and thermal stability greater than 10 years, with discrete germanium diodes as access devices to allow for read/write operations. The crossbar architecture can be extended to multiple layers to create a 3-D stackable, nonvolatile memory with a sub-1F^2 effective cell size.**

***Index Terms*— Diode-MTJ crossbar, magnetic tunnel junction (MTJ), magnetoelectric random access memory (MeRAM), magnetoresistive random access memory (MRAM).**

I. Introduction

MAGNETORESISTIVE RAM (MRAM), using spin-transfer-torque (STT) in magnetic tunnel junctions (MTJs), is a promising emerging memory technology for both embedded and stand-alone applications [1], [2]. STT-MRAM normally uses a 1-transistor/1-MTJ (1T-1MTJ) memory cell structure, with complimentary metal-oxide-semiconductor (CMOS) transistors as the access devices [3]. However, the relatively large currents required to switch STT-based MTJs require fairly large transistors to drive them [4]. Thus, the density of STT-MRAM arrays is often limited not by the dimensions of their MTJs, but rather by the switching current of the MTJ device itself. Additionally, the use of three-terminal CMOS transistors imposes a layout-based limit of 6F^2 on the maximum cell density [5].

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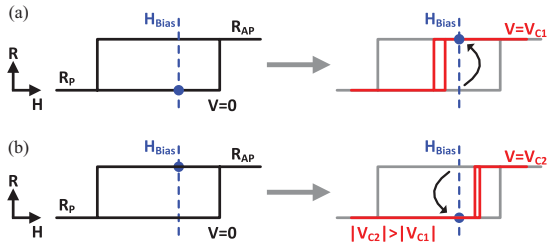

Fig. 1. Writing of the VCMA-based MTJs in the P to AP direction is accomplished by a voltage V_{C1}, which reduces the coercivity of the free layer and results in a single available state at the bias field H_{Bias} provided by the fixed layer. Further increasing the magnitude of the voltage to V_{C2} allows STT to switch the device in the opposite (e.g., AP to P) direction [6], [7].

The use of transistors in STT-MRAM is dictated by its purely current-controlled write mechanism, where currents of opposite polarities are needed to write different bits of information [3], preventing the realization of crossbar arrays with diodes as the access devices. In principle, however, crossbars are the densest memory arrays possible (with a 4F^2 cell size), and hence the realization of a diode-controlled memory cell for crossbar arrays can greatly increase the density and scalability of MRAM [8]. Furthermore, the crossbar architecture allows for 3-D stacking of multiple diode-MTJ memory layers in the CMOS back-end-of-line fabrication steps, increasing the effective density with each layer (2F^2 for two layers, etc.).

In this letter, we report a magnetoelectric (i.e., electric-field-controlled) random access memory (MeRAM) cell that uses voltage-controlled MTJs as the nonvolatile memory elements, with a voltage-controlled magnetic anisotropy (VCMA) switching mechanism, in addition to traditional STT switching [6], [9]–[12]. The use of VCMA and STT allows the MTJ to switch in both directions (write opposite bits of information) using voltages of the same polarity, but with different magnitudes. This enables a diode-MTJ crossbar architecture, with the potential for a sub-1F^2 effective cell size significantly denser than traditional (purely current-switched) STT-MRAM. Experimental validation of a nonvolatile crossbar memory array, leveraging recently developed MTJs [6] with a combined VCMA and STT switching mechanism, is also shown.

II. Memory Operation Principles

Fig. 1 shows how voltage pulses of the same polarity, but different amplitudes, can be used to switch a MeRAM device in opposite directions [6]. The free layer of the MTJ devices is subject to a bias field H_{Bias}, due to the combination of the stray field from the pinned layer, as well as an exter-

nally applied magnetic field (which is fixed throughout the experiment and can be removed in an optimized device by proper design of the fixed layer to apply the required H_{Bias}). This field favors one of the states in the free layer (e.g., AP state in Fig. 1), but is small enough not to compromise the bistability of the bit. This is shown schematically in the resistance R versus magnetic field H curves at equilibrium ($V = 0$) in Fig. 1, where the magnetic field H is along the easy axis of the free layer. Once a voltage V_{C1} of the proper polarity is applied, the modification of the interfacial perpendicular anisotropy via the VCMA effect [9] reduces the coercivity of the free layer, resulting in a single available state at H_{Bias} and, thus, $P \rightarrow$ AP switching in Fig. 1(a). When the voltage is increased to V_{C2}, the coercivity will further decrease, but current-induced effects also become increasingly important. If the polarity is designed such that STT favors the opposite free layer direction compared to the bias field H_{Bias}, a voltage pulse V_{C2} will thus induce AP $\rightarrow$ P switching in Fig. 1(b). This allows for a unipolar set/reset write scheme, where voltage pulses of the same polarity, but different amplitudes, can be used to switch the device between the P and AP states [6], [7].

Notice that this switching scheme can be used in both perpendicular and in-plane MTJs. In perpendicular devices, the coercivity of the free layer can be directly controlled by voltage via the VCMA effect [12], while the coercivity in in-plane devices can be designed to be sensitive to the VCMA effect by tuning the perpendicular anisotropy, such that the free layer is close to the compensation point between in-plane (shape-induced) and out-of-plane (voltage-dependent) magnetic anisotropies [13]. In both cases, in principle, there is no need for external magnetic fields, and the bias field can be provided by the pinned layer. However, the asymmetry of the R-H loop introduced by the unbalanced fixed layer (see Fig. 1) needs to be taken into account when assuring enough thermal stability for the state not favored by H_{Bias} (e.g., P in Fig. 1). Finally, note that voltage pulses of the opposite polarity will not switch the device, but rather reinforce the initial state due to VCMA [6].

Fig. 2(a) and (b) shows the schematic and layout view for one vertical slice of a high-density crossbar memory array using voltage-controlled MTJs. The devices' unipolar set/reset write scheme allows for a diode to be integrated in series without any loss in functionality. The series diode also has the added benefit of eliminating the sneak currents present in traditional crossbar arrays [14]. Also, by eliminating the access transistor present in previous 1T-1MTJ designs, MeRAM can improve memory density with the 3-D stacking of memory layers. A series stacked diode, fabricated on top of the MTJ, means that a $4F^2$ cell can be realized per MeRAM layer.

Similar to other types of MRAM, scaling of (perpendicular) MeRAM devices requires an increase of the perpendicular anisotropy of the free layer to maintain thermal stability. On the other hand, MeRAM does not necessarily place a limit on the current drive capability of its access devices, given that it can operate with currents smaller than purely STT-based memory devices. This is in contrast to STT-MRAM, where density is usually limited by the current drive capability (hence, width) of its access transistors. This can confer a potential scalability advantage to MeRAM.

III. Experiment

A small crossbar memory array was constructed from 190 by 60-nm MTJ nanopillars (corresponding to a 65-nm

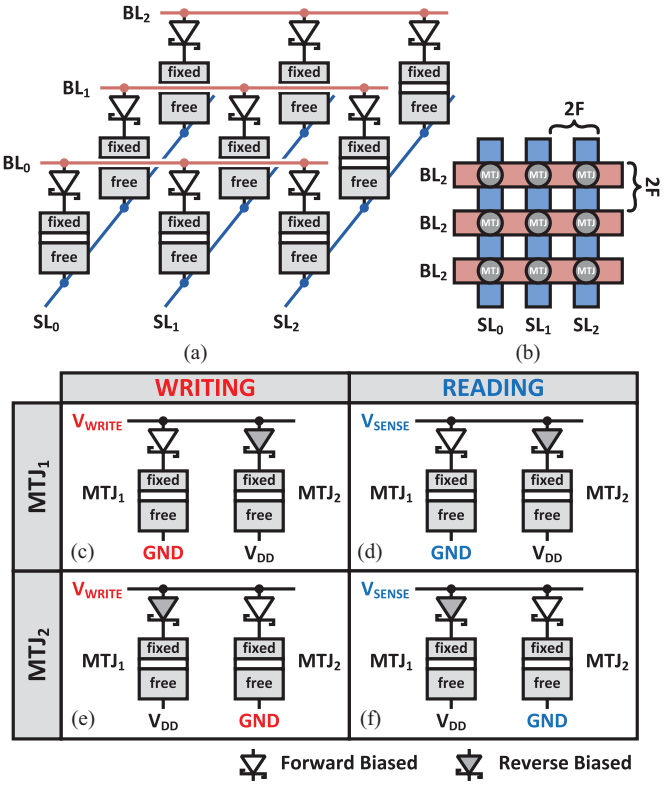

Fig. 2. (a) Schematic and (b) layout views of the crossbar array structure, with integrated diodes, for 3-D MeRAM. The array configuration for reading (d) and (f) and writing (c) and (e) data out of the testing setup.

CMOS technology), with an R_P of 5.8 kΩ, $H_{\mathrm{Bias}} \approx +15$ Oe, and thermal stability $\Delta = E/k_BT > 40$ (where E is the energy barrier between the two MTJ free layer states, k_B is the Boltzmann constant, and T is the operating temperature) for both P and AP states (projected to > 10 years using magnetic-field-dependent switching measurements) at room temperature. The MTJs were connected to discrete germanium diodes ($V_{\mathrm{TH}} = 0.2$ V) used as access devices. The MTJ material stack was sputter deposited using a Singulus TIMARIS PVD system. Devices were fabricated using electron-beam lithography and ion milling techniques from the following stack: Ta(5)/$Co_{20}Fe_{60}B_{20}$ (1.1–Free Layer)/MgO (1.2)/$Co_{60}Fe_{20}B_{20}$ (2.7)/Ru (0.85)/$Co_{70}Fe_{30}$ (2.3)/PtMn (20) (thickness in nm). The thickness of the free layer was designed to be near the compensation between in-plane shape anisotropy and out-of-plane interface anisotropy to maximize the VCMA-induced manipulation over the state of the free layer. However, this compensation also leads to canting of the free layer due to the influence of higher-order anisotropy terms [6], [10], reducing the effective TMR between the equilibrium states of our MTJs to 5%. It is expected that further enhancement of the VCMA effect via materials optimization will mitigate the presence of canted states for our unipolar switching scheme and allow for fully in-plane or perpendicular magnetization with TMR $>$ 100%.

The probability of writing as a function of applied voltage for the MTJs used in the crossbar is shown in Fig. 3, demonstrating their unipolar set/reset characteristics. Data was obtained using 100 repetitions for each voltage with 100-ms pulsewidths. An overlap between the switching peaks is observed, which is expected to be reduced for larger VCMA effect values and would result in improved write noise-margin for the bit cell. Similarly, reducing the reverse-bias

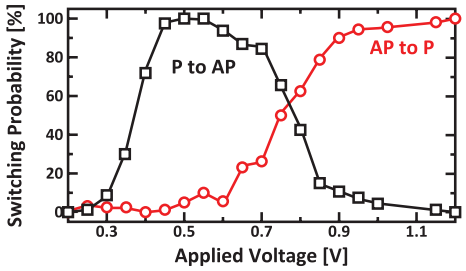

Fig. 3. Measured probability of switching curves for the VCMA-based MTJs. Data is obtained using 100 repetitions for each voltage with 100-ms pulsewidths. The combination of VCMA and STT effects allow for a unipolar set/reset switching scheme with switching voltages 0.5 and 1.1 V, respectively. Measurements on similar devices with a thicker MgO barrier ($\sim$20 times larger resistance) showed only the first (VCMA-induced) switching described in this work, with the second (STT-induced) switching absent at larger voltages.

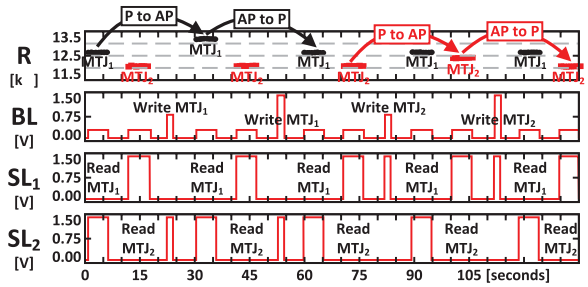

Fig. 4. Measured transient waveforms for reading and writing the crossbar array, demonstrating that MTJ_1 can be written with unipolar set/reset voltages (0.5 and 1.1 V, respectively) and read without disturbing MTJ_2 and vice versa. A sensing voltage of 0.2 V in the SL is used for the read process, while unaccessed SLs are pulled to V_{DD} (1.5 V).

diode leakage current improves the read noise-margin. The configuration of the testing setup for reading and writing the devices in the test array is shown in Fig. 2(c)–(f). During both reading and writing, unaccessed bit-lines (BLs) are grounded while unaccessed source-lines (SLs) are pulled to V_{DD} (1.5 V), reverse biasing the series diode for unaccessed bits. During the write operation, the target SL is pulled to ground, while the target BL is pulsed with the appropriate set/reset voltage, 0.5 and 1.1 V, respectively. During the read operation, the target SL is pulled to ground and the target BL is connected to a sense amplifier. To prevent disturbing the state of the desired bit cell, a sensing voltage of 0.2 V is used. To maximize the read margin of the accessed memory cell, minimizing the forward drop across the access diode is crucial. This is accomplished through the use of low-threshold Schottky (germanium) diodes. The ultimate size of the crossbar array is determined by the reverse bias leakage of the diodes and the resistance of the MTJs. Larger arrays can be built if the resistance of the MTJs is increased or if the leakage current of the diodes is reduced.

Fig. 4 shows experimental transient waveforms demonstrating the functionality of the crossbar memory array. MTJ_1 and MTJ_2 are first initialized into the P state using an external magnetic field. Then, MTJ_1 is switched from P to AP, then back to P, without disturbing the value of MTJ_2. Similarly, MTJ_2 is also switched from P to AP, then back to P, without disturbing the value of MTJ_1. Switching is preformed using voltage pulses of 0.5 and 1.1 V for a period of 1 s. After writing, both MTJ_1 and MTJ_2 are read 20 times using 0.2 V without disturbing the state of the MTJs in the array.

IV. Conclusion

A small diode-MTJ MeRAM crossbar array was experimentally demonstrated. The use of diodes as access devices was enabled by a unipolar set/reset write scheme that simultaneously exploited the VCMA and STT effects. The voltage-controlled diode-MTJ pair can be used in crossbar arrays with a potential $4F^2$ cell size. The MTJ memory layer is compatible with CMOS BEOL fabrication steps. To achieve higher density, by stacking four or more MeRAM layers, a sub-$1F^2$ effective cell size can, in principle, be realized. Additionally, by placing the memory arrays directly over the array decoders and sense-amplifiers, a cell efficiency of nearly 100% can theoretically be achieved.

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