Electrical Stress and Total Ionizing Dose Effects on Graphene-Based Non-Volatile Memory Devices

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***Abstract*—Electrical stress and 10-keV x-ray and 1.8-MeV proton irradiation and annealing responses are evaluated for graphene-based non-volatile memory devices. The memory characteristics of these structures derive primarily from hysteretic charge exchange between the graphene and interface and border traps, similar to the operation of metal-nitride-oxide-semiconductor memory devices. Excellent stability and memory retention are observed for ionizing radiation exposure or constant-voltage stress. Cycling of the memory state leads to a significant reduction in memory window.**

***Index Terms*—Graphene FET, sol-gel PZT, total ionizing dose.**

I. Introduction

DUE to their potentially superior electrical and mechanical properties relative to silicon, carbon based materials are promising candidates for integration into future integrated circuit technologies [1]–[3]. Recently, graphene-based non-volatile field effect transistors (NVFETs) have been developed that combine the speed of graphene with the retention properties of a lead-zirconate titanate (PZT) layer that exhibits anti-hysteretic response [4]–[8]. Due to the high dielectric constant of PZT, the scattering of charged impurities is effectively screened, leading to enhanced carrier mobility in graphene NVFETs [9]. These devices are of significant interest for future non- volatile memory applications.

Initial studies of the response of graphene-based MOS structures to x-ray irradiation have been performed on simple transistor structures and material layers [10], [11]. In this study, we evaluate the response of graphene/PZT NVFETs to 10-keV x-ray irradiation and 1.8-MeV proton irradiation.

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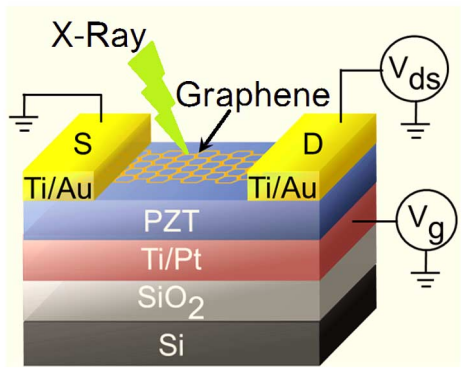

Fig. 1. Schematic cross-section of a graphene NVFET with PZT gate dielectric.

The memory window of the device remains essentially unchanged through 1 Mrad(SiO_2) radiation exposure, with a small positive shift in current-voltage characteristics that is consistent with negatively charged surface states on the graphene layer after x-ray irradiation. The maximum current increases with proton irradiation and post-irradiation annealing; the memory window decreases with proton irradiation and recovers after annealing. Devices are found to be sensitive to memory window reduction with cycling.

II. Experimental Details

A single-layer graphene NVFET structure is shown schematically in Fig. 1. CVD graphene was grown on a Cu foil and then transferred to a PZT-Pt/Ti-SiO_2-Si substrate. The ferroelectric PZT layer was deposited via a sol-gel process. The thicknesses of the PZT layer and SiO_2 buffer layer are 51 nm and 500 nm. The rms surface roughness of the PZT layer is $\sim$ 2 nm. The 100 nm/10 nm Pt/Ti layer underneath the PZT serves as the gate electrode. The thickness of source/drain Ti/Au layer is 10 nm/90 nm. The Raman data in [7] confirm the high quality of the single-layer-graphene films of these development stage devices. Additional process details are provided in [6], [7]. During measurement, the source-drain voltage V_{ds} was kept at 5 mV, while the gate voltage was swept from negative to positive and then positive to negative. The drain current I_D was repeatable after each sweep.

In this work, we have tested devices with varying gate lengths ranging from 30 μm to 3 μm and gate widths ranging from 10.5 μm to 4.5 μm. Data shown in this work were selected as representative responses from out of at least three samples for each experimental condition.

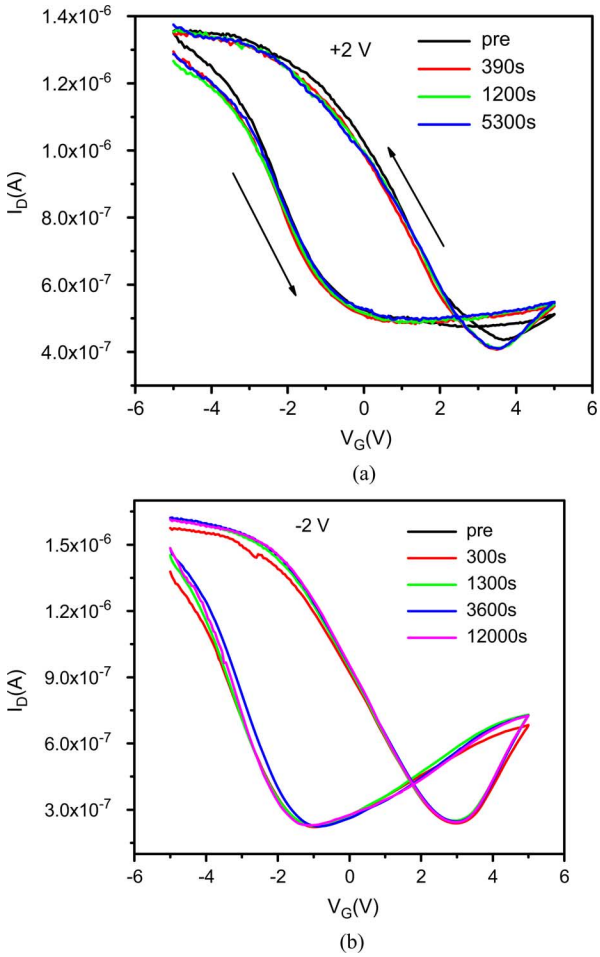

Fig. 2. Drain current (I_D) versus gate voltage (V_G) as a function of stress time for (a) positive gate bias $+2$ V on a device of width/length ratio (W/L) $=$ 10.5 μm/3 μm and (b) negative gate bias -2 V on a device of W/L $=$ 10.5 μm/9 μm.

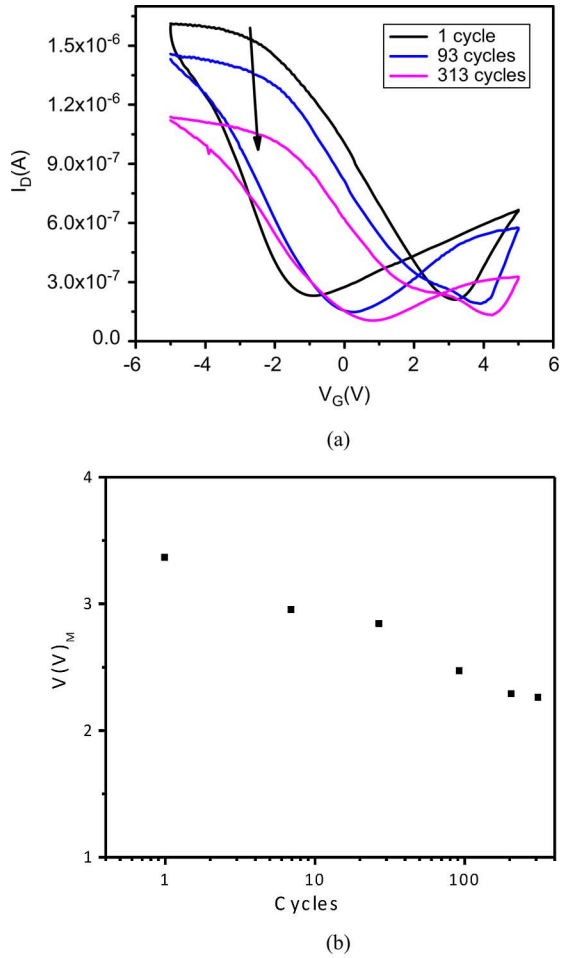

Fig. 3. (a) Drain current I_D as a function of gate voltage V_G after cycles (b) Memory window V_M as function of cycle times on devices of channel W/L $=$ 10.5 μm/30 μm.

The graphene NVFETs were irradiated at the wafer level with a 10-keV x-ray source at a dose rate of 31.5 krad(SiO_2)/min at room temperature with applied gate biases of 2 V and -2 V. Device responses to biased annealing after x-ray irradiation exposure were evaluated in-situ at room temperature. The proton irradiation was performed with a 1.8-MeV source in vacuum at varying fluences with the gates grounded and other terminals floating. Post-irradiation annealing was performed in air at room temperature. Device characterization was performed in air with a HP 4156A Semiconductor Parameter Analyzer.

III. Electrical Stress

A. Constant Voltage Stress

Fig. 2 shows the drain current I_D at V_D $=$ 5 mV versus gate voltage V_G for a graphene NVFET as a function of constant-voltage stressing time for (a) $+2$ V and (b) -2 V applied gate bias. In order to characterize the device response, the drain-to-source bias V_{ds} was held at 5 mV while the gate voltage was swept from -5 V to 5 V and then 5 V to -5 V. In a graphene NVFET, the memory window (ΔV_M) can be defined as the difference in V_G that occurs at the current value corresponding to the midpoint of the maximum and minimum possible current of the device [7]. Very little change in memory window is observed with either positive or negative constant voltage stress.

The direction of the hysteresis loop is denoted in Fig. 2(a). Note that the observed direction of the hysteresis is opposite to the expected polarization direction of the PZT. This behavior is referred to as "anti-hysteresis" in [4], [7], [8], and indicates that memory storage in these devices is dominated by charge exchange between the graphene layer and interface and border traps [12], [13], as opposed to ferroelectric switching [14]–[16]. One possible reason for this response is that the bulk polarization can be screened by charged surface adsorbates from water molecules located between PZT and graphene [4], [17]. In addition, there is evidently a significant density of defects at or near the PZT/graphene interface [7], [8]. When the gate voltage increases, electrons are captured by interface and border traps. When the sweep direction is reversed, the trapped electrons at or near the interface modify the charge concentration in the graphene, leading to an increase in current and a shift in threshold voltage, as observed in Fig. 2. This simple trapping mechanism is quite similar to typical memory programming in metal (or silicon)-nitride-oxygen-Si, MNOS or SNOS, memories [18], [19]. Assuming the effective dielectric constant $k \approx 400$ [7], the memory window of ~ 4 V is consistent with charge trapping at or near the interface $\sim 5 \times 10^{13}/\text{cm}^{-2}$.

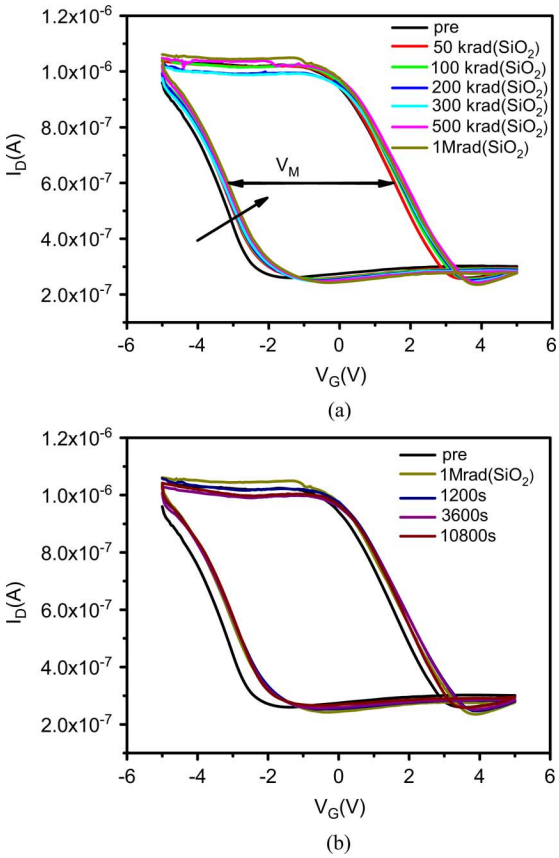

Fig. 4. Drain current I_D as a function of gate voltage V_G and (a) varying total dose with applied gate bias of $+2$ V and (b) annealing time with applied gate bias of $+2$ V on devices of channel $W/L = 10.5\ \mu\text{m}/9\ \mu\text{m}$.

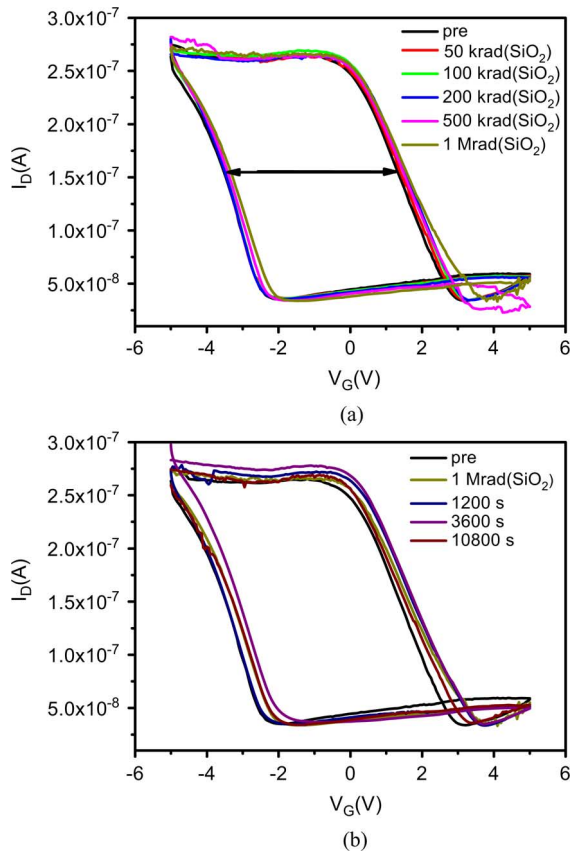

Fig. 5. Drain current I_D as a function of gate voltage V_G and (a) varying total dose with applied gate bias of -2 V and (b) annealing time with applied gate bias of -2 V on devices of channel $W/L = 4.5\ \mu\text{m}/3\ \mu\text{m}$.

B. Cycling

The reliability of of the graphene NVFET structures was evaluated for unirradiated devices at room temperature in air, with the results shown in Fig. 3. In Fig. 3(a), a sequence of $I_D - V_G$ characteristics is shown for a representative device after numerous cycles. The maximum current decreases $\sim 27\%$ after 300 cycles. The memory window V_M is plotted in Fig. 3(b). V_M degrades to $\sim 33\%$ of the original value after 300 cycles. This is similar to ferroelectric fatiguing, in which a portion of the trapped charge can be swept into the impurity-related point defects in PZT [20]. The loss of carriers in the graphene layer will result in the degradation of both conducting current and memory window.

IV. Irradiation and Annealing

A. 10-keV X-ray Irradiation and Annealing

Fig. 4 shows the drain current I_D versus gate voltage V_G as a function of total ionizing dose and annealing time at room temperature. The devices were irradiated up to 1 Mrad(SiO_2) at a gate bias of $+2$ V, with all other terminals grounded. The maximum current increases slightly and the minimum current decreases with total dose. The overall small positive shift of the characteristics in Fig. 4(a) is consistent with radiation-induced generation of reactive oxygen species, which can introduce electron traps on the surface of graphene [10]. Based on the relative sizes of the positive shift (small) and the hysteresis (large), charge trapping at interface traps and border traps in the PZT appears to have a more significant effect on the device operating characteristics [12] than surface O atom adsorption in the graphene [10]. The radiation tolerance of PZT-based ferroelectric memory devices on Si has been reported in [14]–[16], and that of SNOS memories has been described in [19]. Each type of memory is typically total-ionizing-dose tolerant, consistent with the lack of additional, significant stable trapping after TID exposure here. Fig. 4(b) shows the results of annealing the irradiated device at room temperature for up to 3 hours under the same applied bias conditions as in Fig. 4(a). The annealing was done in-situ at room temperature. A post-irradiation recovery in maximum current was observed for the radiation-induced degradation through biased-anneal, without significant voltage shifts. The recovery in current-voltage characteristic can result from the partial neutralization of trapped charge within the PZT layer [14]–[16].

Fig. 5 shows the $I_D - V_G$ characteristics as a function of total ionizing dose and annealing time at a gate bias of -2 V. Similar degradation was found for negative bias conditions as for positive bias in Fig. 4. The increased current for these devices, compared to Fig. 4, is primarily because $W/L = 4.5\ \mu\text{m}/3\ \mu\text{m}$ for Fig. 5 and $W/L = 10.5\ \mu\text{m}/9\ \mu\text{m}$ for Fig. 4. The device responses are otherwise similar. The hysteresis loop shifts positively after irradiation. The internal field can be changed by radiation-induced trapped charge in the near-interfacial layers,

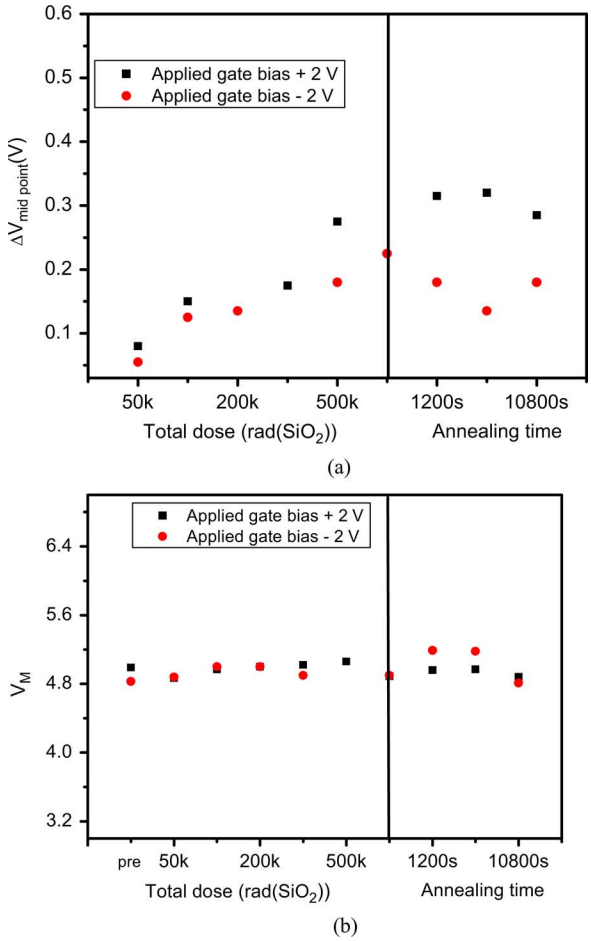

Fig. 6. (a) Voltage at midpoint shift $\Delta V_{\mathrm{midpoint}}$ and (b) memory window ΔV_{M} as a function of x-ray dose and annealing time with applied gate bias of $+2$ V and -2 V on devices of $W/L = 10.5\ \mu\mathrm{m}/9\ \mu\mathrm{m}$ and $W/L = 4.5\ \mu\mathrm{m}/3\ \mu\mathrm{m}$ at room temperature.

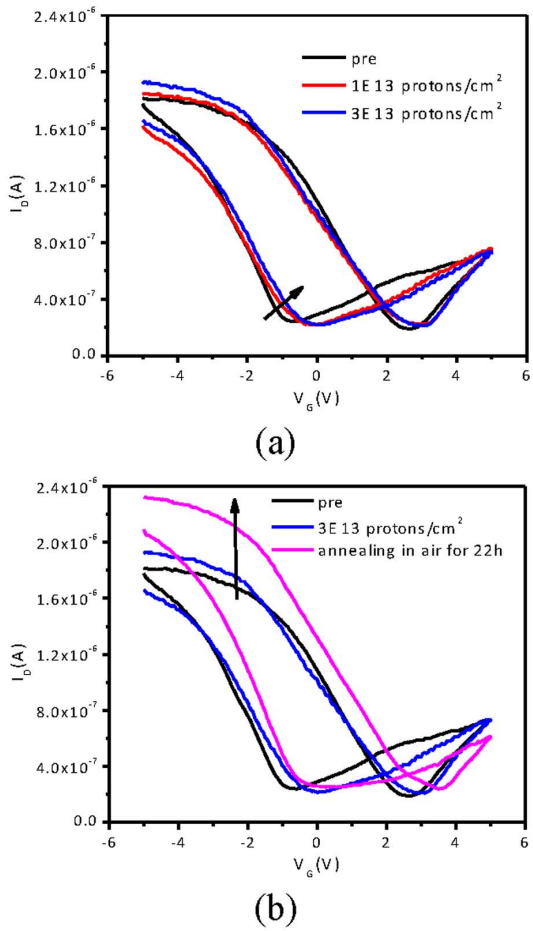

Fig. 7. Drain current I_D as a function of gate voltage V_G (a) at varying fluences with gate grounded and other terminals floating and (b) after annealed in the air on devices of channel $W/L = 7.5\ \mu\mathrm{m}/3\ \mu\mathrm{m}$.

leading to a distortion of the shapes of the hysteresis curves in Figs. 4 and 5 [14], [21], [22].

The shift of the midpoint voltage is shown in Fig. 6(a). Qualitatively similar responses were observed for positive and negative radiation biases. Positive gate bias results in slightly more charge trapping than negative bias [16]. No obvious annealing behavior was found for the case of positive gate bias; however, for annealing under negative bias, holes accumulate at the interface to compensate the electrons that are trapped at the interface during irradiation. For longer time annealing under negative gate bias, surface O atom adsorption [10] evidently causes the mid-point voltage to increase, reversing this trend.

The memory window dependence on total dose and annealing time is shown in Figs. 6(b). No significant change in memory window with total dose or annealing time is observed. Hence, the charge trapping within the PZT is not enough to affect the charge trapping at the near interface of PZT/graphene; the trapped charge only shifts the center of the operating voltage range slightly, for 10-keV x-ray doses up to 1 Mrad(SiO_2).

B. 1.8 MeV Proton Irradiation and Annealing

1.8-MeV proton irradiation also was performed on unlidded, packaged devices in vacuum at room temperature. During the proton irradiation, the gate is grounded, with other terminals floating. The initial memory window is similar for these devices ($W/L = 4.5\ \mu\mathrm{m}/6\ \mu\mathrm{m}$) and those of Fig. 4 ($W/L = 10.5\ \mu\mathrm{m}/9\ \mu\mathrm{m}$). Five devices were exposed to proton irradiation with similar results. Fig. 7 shows the $I_D - V_G$ characteristics (a) as a function of fluence and (b) for post-irradiation annealing, with the gate grounded. The midpoint voltage shifts to the right and the maximum current increases with fluences up to 3×10^{13} protons/cm^2. The memory window decreases with fluence in this case, in contrast to the smaller changes that occur during x-ray irradiation (Figs. 4 and 5). If this were due to purely ionization effects, the charge trapping in the near-interfacial PZT layer observed after 3×10^{13} protons/cm^2 should be greatly enhanced compared to 1 Mrad(SiO_2) x-ray irradiation, because of the higher effective dose delivered to the insulator, ~ 60 Mrad(SiO_2) for the 1.8 MeV proton irradiation [23]. The degradation of the memory window represents the suppression of charge exchange between the graphene layer and border traps. It is likely that the occupancy of the border traps can be increased by radiation-induced charges, limiting exchange sites for induced carriers from the graphene layer. Because the irradiation is performed in vacuum, degradation of the surface due to O adsorption does not occur, in contrast to X-ray irradiation in air [10].

In Fig. 7(b), post-irradiation annealing in air was performed. The memory window shows slight recovery after 22 h, which

is consistent with responses observed for irradiated PZT capacitors in [14]–[16]. The maximum current continues to increase with both proton irradiation and annealing. The increase during proton irradiation is likely due to the compensation of border traps, consistent with the reduction of the memory window, and the continuing increase during annealing likely results from O adsorption as the graphene surface is exposed to air [10], [24]. Additional research is required to evaluate the contributions of these and other potential mechanisms that may affect the response of graphene NVFETs to electrical response and radiation exposure.

V. Summary and Conclusions

We have investigated the responses of graphene NVFET memory devices to electrical stress and 10-keV x-ray and 1.8 MeV proton irradiation and annealing. The non-volatile memory characteristics derive from the charge exchange between the PZT layer and the graphene film. No significant change in memory window is observed with ionizing irradiation or constant voltage stress. The maximum current increases after both proton irradiation in vacuum as a result of the passivation of border traps by radiation-induced charge, and during annealing in air by the increased hole concentration in the graphene produced by the electrostatic effects of surface charge. Cycling of the memory states leads to a reduction of the memory window. These results emphasize that the oxygen concentrations in the environment surrounding graphene NVFETs are important considerations in determining their radiation response and long-term reliability.

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