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Fabrication and Electrical Characteristics of Graphene-based Charge-trap Memory Devices

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Graphene-based non-volatile charge-trap memory devices were fabricated and characterized to investigate the implementation effect of both 2-dimensional graphene and the 3-dimensional memory structure. The single-layer-graphene (SLG) channel devices exhibit larger memory windows compared to the multi-layer-graphene (MLG) channel devices. This originates from the gate-coupling strength being larger in SLG devices than in MLG devices. Namely, the electrostatic charge screening effect becomes enhanced upon increasing the number of graphene layers; therefore, the gate tunability is reduced in MLG compared to SLG. The results suggest that SLG is more desirable for memory applications than MLG.

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I. INTRODUCTION

The solid-state memory drive (SSMD) has attracted much attention as a mainstream module for data storage in next-generation electronic-device platforms [1,2]. The majority of current SSMDs, however, utilize conventional Si complementary metal-oxide-semiconductor (CMOS) transistor-based non-volatile memory cells that suffer from the scaling limit and its parasitic short-channel effects.

Recently, graphene has been considered as one of the potential candidates for future electronic devices because of its outstanding electrical properties. Particularly, the 2-dimensionality of graphene can allow scaling beyond the CMOS technology; in addition, the ambipolar carrier conduction with no charge depletion in graphene can resolve the short-channel-effects in CMOS devices. Furthermore, if a 3-dimensional memory structure is implemented in the graphene-based memory device, the memory performance as well as the memory capacity can be maximized; *e.g.*, the reduced cell-to-cell interference in graphene floating-gate memories [3], the enhanced gate-coupling in ferroelectric memories with graphene channels [4,5], and the enlarged memory windows in charge-trap memories with graphene channels [6]. In other words, a combination of both 2-dimensional graphene and a 3-dimensional memory structure could be beneficial for future SSMDs that require integration of smaller, lighter, and faster memory and logic elements. Moreover, recent advances in the large-scale growth of both single-layer-graphene (SLG) and multi-layer-graphene (MLG) [7,8] provide ample opportunities for the demonstration of graphene-based SSMDs.

In this research, we fabricated graphene-based non-volatile charge-trap flash memory (NV-CTFM) devices and investigate their electrical characteristics. The NV-CTFMs were fabricated in the form of a graphene-channel field-effect-transistor (gFET) with a charge-storage stack of $Al_2O_3/HfO_x/Al_2O_3$ (AHA). In order to examine the memory performance of AHA-gFETs as NV-CTFMs, we systematically analyzed the memory performances of both SLG and MLG AHA-gFETs. The results of the in-

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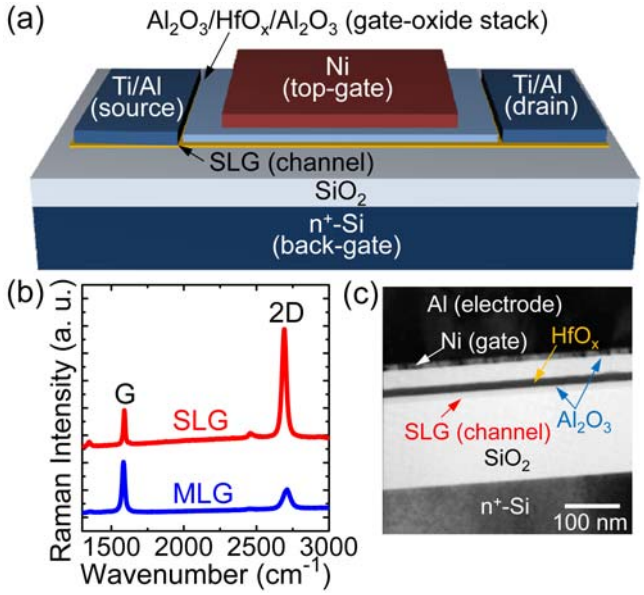

Fig. 1. (Color online) (a) Schematic illustration of the AHA-gFET structure. (b) Raman spectra of the SLG and MLG transferred onto SiO_2 layers. (c) Cross-sectional TEM image of a SLG AHA-gFET across the Ni/AHA/SLG/SiO_2/n^+-Si.

depth analyses on the operation schemes, memory window (ΔV_M), retention characteristics, and cumulative distributions are discussed.

II. EXPERIMENTAL DETAILS

The device structure of NV-CTFM is schematically illustrated in Fig. 1(a). First, SLG and MLG are grown on Cu and Ni films, respectively, by using chemical vapor deposition [9]. Then, SLG and MLG are transferred onto SiO_2 (100 nm)/n^+-Si substrates. As shown in Fig. 1(b), SLG exhibits a high ratio of 2D/G Raman modes ($\gg$2) while MLG shows a low ratio of 2D/G ($\ll$2). This confirms that SLG is uniformly formed with one atomic layer and that MLG has a few layers [10–12]. After the transfer step, SLG and MLG channels are patterned by using photolithography and are etched by using an oxygen plasma. Then, the Ti/Al source and drain electrodes are formed by using e-beam evaporation and lift-off. Next, a thin Al layer of 10 Å is deposited and oxidized in air to provide Al_2O_3 nucleation sites for subsequent atomic-layer deposition (ALD) of the gate-oxide stack [13]. The triple stack of high-k dielectric AHA (70/70/330 Å) is subsequently deposited by using ALD. Finally, Ni gate electrodes are formed by using a standard lift-off process. Here, the large work-function metal - Ni - is used to reduce the electron back-injection during the erase operation mode of AHA-gFET memory devices [6]. The cross-sectional transmission electron microscopy (TEM) image shows that the as-fabricated AHA-gFET is composed of a clear layered-structure (Fig. 1(c)).

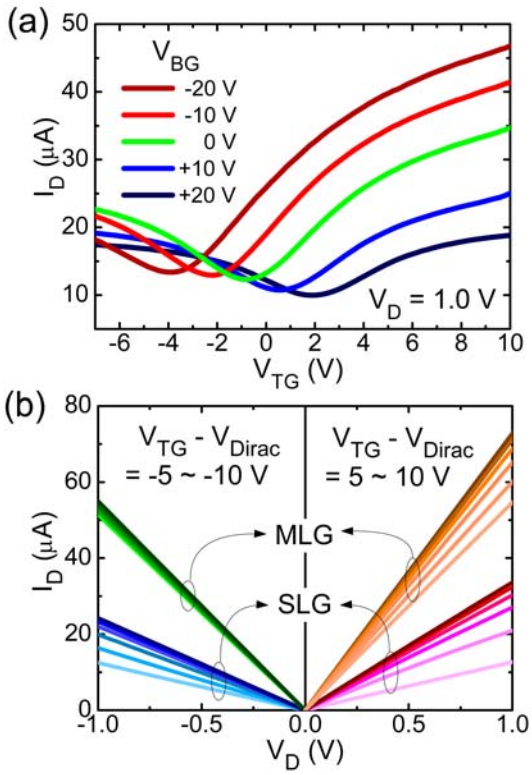

Fig. 2. (Color online) (a) I_D-V_{TG} characteristic curves at various V_{BG} of the SLG AHA-gFET. (b) I_D-V_{DS} characteristic curves at various gate-bias conditions ($V_{G(normal)} = V_{TG} - V_{Dirac}$) of SLG and MLG AHA-gFETs.

III. RESULTS AND DISCUSSION

The drain current *vs.* top-gate voltage (I_D-V_{TG}) characteristic curves at various back-gate voltages (V_{BG}) of the SLG AHA-gFET are shown in Fig. 2(a). The device displays typical V-shaped I_D-V_{TG} curves regardless of V_{BG}. The charge-neutrality point (V_{Dirac}) is clearly seen to vary with V_{BG}; *i.e.*, V_{Dirac} increases when $+V_{BG}$ increases, and *vice versa* for $-V_{BG}$. This is indicative of back-gate tunability for controlling the Fermi potential in SLG. Therefore, one can confirm that the device operates as an FET with ambipolar carrier-conduction properties. For the MLG AHA-gFET, a similar behavior was observed (data not shown).

After observing the back-gate tunability, we also examined the top-gate modulation in the devices because the memory characteristics of NV-CTFMs rely on the top-gate performance. Figure 2(b) shows the drain voltage (V_D)-dependent I_D curves at various V_{TG} bias conditions for both SLG and MLG AHA-gFETs. Here, we note that the normalized top-gate biases (*i.e.*, $V_{G(normal)}$

= V_{TG} – V_{Dirac}) are applied to compare the gate-coupling strengths for both SLG and MLG AHA-gFETs because SLG and MLG devices exhibit different V_{Dirac} positions from each other (see also Figs. 3(a) and 3(b)). As shown in Fig. 2(b), both samples clearly reveal ambipolar characteristics. Here, it should be noticed that the SLG AHA-gFET shows a lower I_D and reveals a stronger gate-coupling strength than the MLG device. The lower I_D in SLG than MLG is attributed to the lower channel conductance due to both the different band-structures in the materials and the thinner cross-section of SLG than MLD. Since SLG has a linear dispersion relationship with zero-energy gap while MLG has a semi-metal band structure [14], the material conductivity of SLG is smaller than that of MLG. Moreover, the thinner cross-section of SLG increases the channel resistance. The thinnest atomic thickness and the linear dispersion relationship of SLG are also responsible for the gate-coupling being stronger in SLG than in MLG. When the cross-sectional channel dimension becomes small, the capacitive coupling around the channel is increased because the electrostatic charge screening at the channel/oxide interface decreases [15,16]. In graphene, the electrostatic screening at the interfacial graphene-graphene layer will also increase when the number of graphene layers increases. In addition, the gate modulation of the Fermi potential will become difficult when the number of graphene layers exceeds a few layers (>2 layers). Therefore, the atomic thickness and the linear dispersion relationship of SLG lead to a greater gate-coupling in SLG AHA-gFETs than in MLG AHA-gFETs.

In NV-CTFMs, the gate-coupling strength directly affects the memory performance because the programming/erasing operation is intimately related to the carrier injection/ejection process through the gate bias. Thus, to evaluate the memory functionality of SLG and MLG g-FETs, we applied the voltage stresses for performing the program/erase operations. In the SLG AHA-gFET, V_{Dirac} appears at ∼−2 V when no programming/erasing voltage ($V_{P/E}$) is applied (Fig. 3(a)). After V_P of +30 V is applied, V_{Dirac} is positively shifted, resulting from a reduction of the electrochemical potential (μ) in the AHA gate stack due to electron injection to AHA . When V_E of −25 V is applied, V_{Dirac} shifts toward the negative direction because of the increase of μ in the AHA due to hole injection from SLG to AHA [6]. A similar feature occurs in the MLG AHA-gFET, as shown in Fig. 2(b). However, the transconductance of the MLG AHA-gFET is smaller than that of the SLG device because of the weaker gate-coupling in MLG than SLG (*i.e.*, the slope of V-shape in SLG is steeper than that in MLG.).

Compared to conventional CMOS memory devices, in graphene-based NV-CTFMs, the memory window (ΔV_M) can be enlarged owing to the ambipolar conduction property [6]. In other words, ΔV_M in gFET memories can be defined as a summation of both the positive maximum ΔV_{Dirac} after a program operation and the negative maximum ΔV_{Dirac} after an erase operation (*i.e.*, $\Delta V_M = |+\Delta V_{Dirac(max)}|V_P| + |-\Delta V_{Dirac(max)}|V_E|$). As indicated in Figs. 3(a) and 3(b), the SLG AHA-gFET shows a larger memory window ($\Delta V_M \sim$ 11.5 V) than the MLG AHA-gFET ($\Delta V_M \sim$ 7.3 V). This indicates that the gate-coupling strength plays a key role for the memory functionality in graphene-based NV-CTFMs, as discussed earlier. To make the impact of gate-coupling on ΔV_M more evident, we compare the ΔV_M for both SLG and MLG AHA-gFETs as functions of $|V_{P/E}|$ (Fig. 4). When $|V_{P/E}|$ increases, ΔV_M monotonically increases in both cases. However, in comparison with the MLG device, the variation of ΔV_M in the SLG AHA-gFET becomes larger as $|V_{P/E}|$ increases. This corroborates the above hypothesis that a high gate-coupling strength is crucial for the memory characteristics of graphene-based NV-CTFMs.

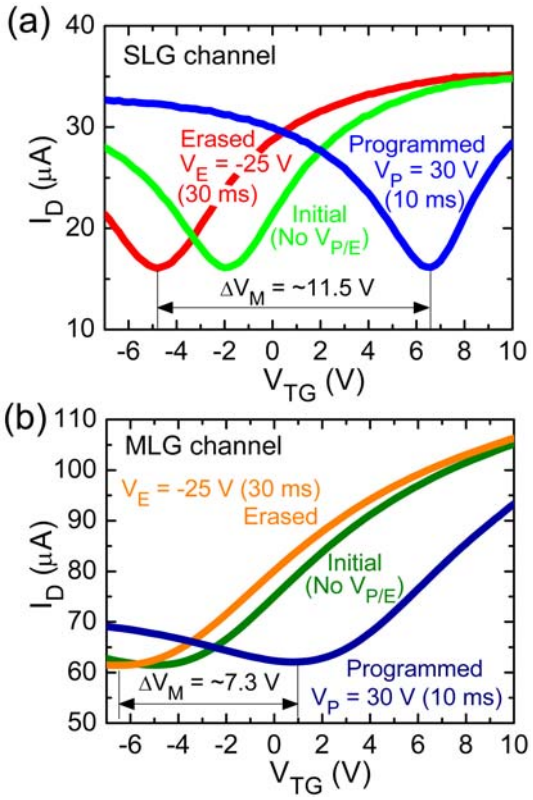

Fig. 3. (Color online) Program and erase operations of (a) SLG and (b) MLG AHA-gFETs. Samples were programmed by using a voltage stress with V_P = 30 V for 10 ms and were erased by V_E = −25 mV for 30 ms.

In the application point of view, the cumulative distributions of key device-parameters are important to estimate the stability for the integration as well as the efficacy of the devices. In Fig. 5(left), the values of V_{Dirac} at the initial state for both SLG and MLG AHA-gFETs are shown. V_{Dirac} is almost identical at −2 V for SLG AHA-gFETs while V_{Dirac} of MLG AHA-gFETs is dis-

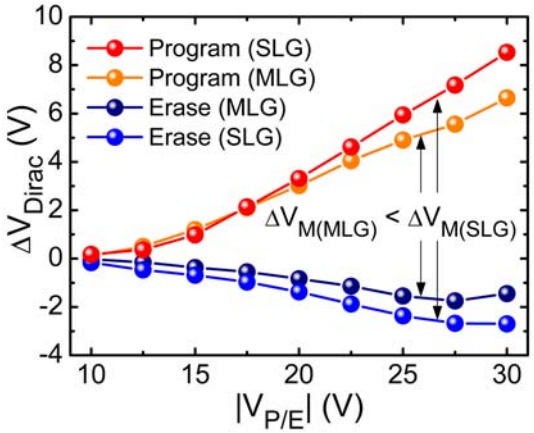

Fig. 4. (Color online) ΔV_{Dirac} as a function of $|V_{P/E}|$ for SLG and MLG AHA-gFETs. The pulse time for both programming and erasing was 10 ms.

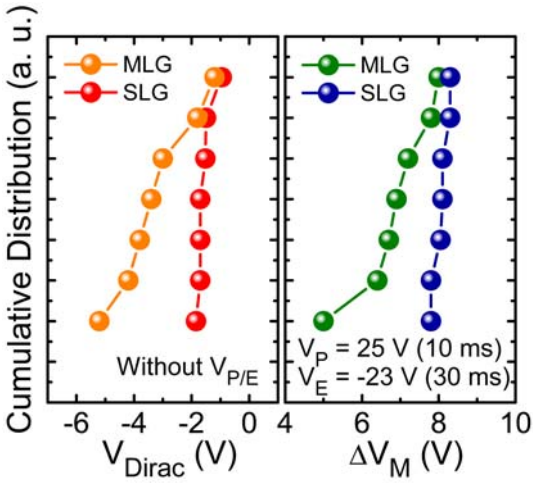

Fig. 5. (Color online) Cumulative distributions of V_{Dirac} (left-hand-side panel) and ΔV_M (right-hand-side panel) for multiple AHA-gFETs with SLG and MLG channels. V_{Dirac} values were obtained from the I_D-V_{TG} curves at the initial states (*i.e.*, no $V_{P/E}$), and ΔV_M values were determined from the I_D-V_{TG} curves under programmed and erased states. For programming and erasing, the voltage stresses of $V_P = 25$ V for 10 ms and $V_E = -23$ mV for 30 ms were applied, respectively.

tributed over a wide voltage range (−1.5 – −5.5 V). Similarly, ΔV_M of MLG AHA-gFETs is random whereas SLG AHA-gFETs display an almost identical ΔV_M of ∼8 V (Fig. 5(right)). The large variations in both V_{Dirac} and ΔV_M for MLG AHA-gFETs are presumably due to the non-uniform layer-thickness of MLG. Currently, a uniform coverage of MLG over a large area is still challenging. Thus, to improve the memory functionality of MLG-based memory devices, further optimization of large-area MLG growth is required.

The above features were also observed to influence the data retention characteristics. The SLG AHA-gFET can

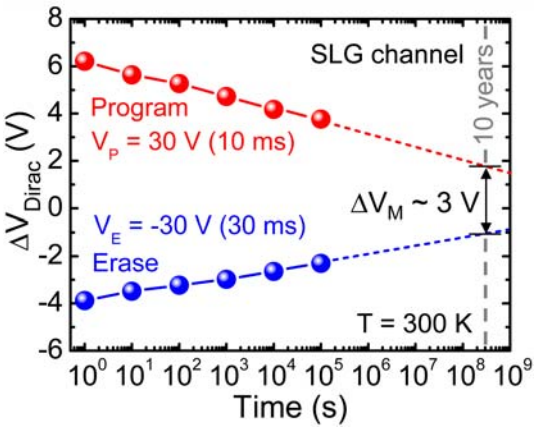

Fig. 6. (Color online) Data retention characteristics of the SLG AHA-gFET. The sample was programmed by using a voltage stress with $V_P = 25$ V for 10 ms and was erased by $V_E = -30$ mV for 30 ms.

maintain its ΔV_M of ∼3 V after 10 years; *i.e.*, the device exhibits ∼33.3% data retention per 10 years at room temperature (Fig. 6). In the case of MLG AHA-gFETs, however, data retention was quite unstable (data not shown). We ascribe the poor retention characteristics in MLG AHA-gFETs to the rough interface between MLG and Al_2O_3 because the number of layers (*i.e.*, thicknesses) of MLG is inhomogeneous over the whole area. Based on the above results, therefore, we can suggest that SLG AHA-gFETs are more desirable for high-fidelity memory devices, although MLG has lower resistivity and is more robust under harsh process conditions.

IV. CONCLUSION

Graphene-based NV-CTFM devices were fabricated in the form of AHA-gFETs by using SLG and MLG. In comparison with the MLG devices, the SLG AHA-gFETs exhibited larger memory windows with reasonable retention characteristics that were almost identical for multiple devices. This is attributed to the gate-coupling strength being greater in SLD devices than in MLG devices, which originates from the reduced electrostatic screening and/or non-metallic ambipolar-carrier-transport properties in SLG. Compared with MLG, the uniform and homogeneous thickness of SLG over the entire substrate is advantageous for yielding identical devices with better retention characteristics. The results suggest that SLG is more efficient for high-fidelity memory devices than MLG.

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