LETTERS

High-speed graphene transistors with a self-aligned nanowire gate

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Graphene has attracted considerable interest as a potential new electronic material[1–11]. With its high carrier mobility, graphene is of particular interest for ultrahigh-speed radio-frequency electronics[12–18]. However, conventional device fabrication processes cannot readily be applied to produce high-speed graphene transistors because they often introduce significant defects into the monolayer of carbon lattices and severely degrade the device performance[19–21]. Here we report an approach to the fabrication of high-speed graphene transistors with a self-aligned nanowire gate to prevent such degradation. A Co_2Si–Al_2O_3 core–shell nanowire is used as the gate, with the source and drain electrodes defined through a self-alignment process and the channel length defined by the nanowire diameter. The physical assembly of the nanowire gate preserves the high carrier mobility in graphene, and the self-alignment process ensures that the edges of the source, drain and gate electrodes are automatically and precisely positioned so that no overlapping or significant gaps exist between these electrodes, thus minimizing access resistance. It therefore allows for transistor performance not previously possible. Graphene transistors with a channel length as low as 140 nm have been fabricated with the highest scaled on-current (3.32 mA μm^{-1}) and transconductance (1.27 mS μm^{-1}) reported so far. Significantly, on-chip microwave measurements demonstrate that the self-aligned devices have a high intrinsic cut-off (transit) frequency of f_T = 100–300 GHz, with the extrinsic f_T (in the range of a few gigahertz) largely limited by parasitic pad capacitance. The reported intrinsic f_T of the graphene transistors is comparable to that of the very best high-electron-mobility transistors with similar gate lengths[10].

With the highest carrier mobility, exceeding 200,000 $cm^2 V^{-1} s^{-1}$ (ref. 8), and many other desirable properties, including a large critical current density ($\sim 2 \times 10^8$ A cm^{-2} (ref. 22)) and a high saturation velocity (5.5×10^7 cm s^{-1} (ref. 11)), graphene has significant potential for high-speed electronics to offer excellent radio-frequency characteristics with very high cut-off frequency (f_T). Importantly, recent studies have demonstrated graphene transistors operating in the gigahertz regime[12–14,16–18] with a record of f_T = 100 GHz (ref. 13). However, the reported radio-frequency performance so far is still far from the potential that the graphene transistors may offer, and is primarily limited by two adverse factors in the device fabrication process.

The first limitation is associated with the severe mobility degradation resulting from the graphene–dielectric integration process, which introduces substantial defects into pristine graphene lattices[20,23]. To overcome this, we have recently developed a strategy to integrate high-quality, high-dielectric-constant dielectrics with graphene using a physical assembly approach without introducing any appreciable defects into the graphene lattices, and have demonstrated top-gated graphene transistors with carrier mobilities exceeding 20,000 $cm^2 V^{-1} s^{-1}$ (refs 24–26). Another limitation of the top-gated graphene transistors reported until now is the large access resistance due to non-optimum alignment of the source, drain and gate electrodes, which can have particularly adverse effects on short-channel devices. With decreasing channel length, there is an increasing demand for a more precise device fabrication process. In state-of-the-art silicon metal–oxide–semiconductor field-effect transistor (MOSFET) technology, a self-aligned gate structure is used to ensure that the edges of the source, drain and gate electrodes are precisely positioned so that no overlapping or significant gaps exist between them. However, these conventional dielectric integration and device fabrication processes cannot be readily used for graphene-based electronics, as many of them can lead to significant damage to the monolayer of graphene lattices, resulting in severe performance degradation.

Here we report a new strategy to fabricate graphene transistors using a Co_2Si–Al_2O_3 core–shell nanowire as the self-aligned top-gate (Fig. 1). To make the device, graphene flakes were first mechanically peeled onto a highly resistive silicon substrate (>18,000 Ω cm) with a 300-nm-thick layer of thermal silicon oxide. The Co_2Si–Al_2O_3 core–shell nanowires were aligned on top of the graphene through a physical dry transfer process[24–26], followed by electron-beam lithography, buffered oxide etching to remove the Al_2O_3 shell and expose the Co_2Si core, and a metallization (titanium (70 nm)/gold (50 nm)) process to define the external source, drain and gate electrodes. A thin layer of platinum (10 nm) was then deposited on top of the graphene across the Co_2Si–Al_2O_3 core–shell nanowire, such that the nanowire separates the platinum thin film into two isolated regions that form the self-aligned source and drain electrodes precisely positioned next to the nanowire gate. In this device, the Co_2Si–Al_2O_3 core–shell

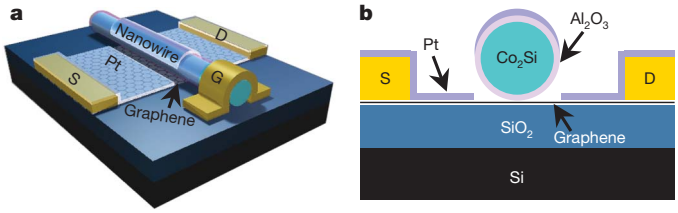

Figure 1 | Schematic illustration of a high-speed graphene transistor with a Co_2Si–Al_2O_3 core–shell nanowire as the self-aligned top-gate. a, Schematic of the three-dimensional view of the device layout. D, drain; G, gate; S, source. **b**, Schematic of the cross-sectional view of the device. In this device, the Co_2Si–Al_2O_3 core–shell nanowire defines the channel length, with the 5-nm Al_2O_3 shell functioning as the gate dielectrics, the metallic Co_2Si core functioning as the self-integrated local gate and the self-aligned platinum thin-film pads functioning as the source and drain electrodes.

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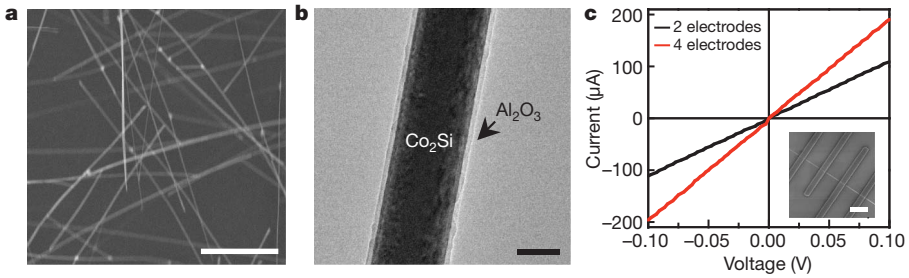

Figure 2 | Characterization of Co_2Si and Co_2Si–Al_2O_3 core–shell nanowires. **a**, Scanning electron microscope (SEM) image of the Co_2Si nanowires. The nanowires were synthesized through a chemical vapour deposition process, with diameters typically in the range of 100–300 nm and lengths of around 10 μm. Scale bar, 3 μm. **b**, TEM image of a Co_2Si–Al_2O_3 core–shell nanowire showing a uniform coating of amorphous Al_2O_3 surrounding the single-crystal Co_2Si core. Scale bar, 50 nm. **c**, Current–voltage characteristics of a single Co_2Si nanowire in two- and four-terminal measurements, used to determine the nanowire resistance and resistivity. Inset, SEM image of the device; scale bar, 3 μm.

nanowire defines the channel length, with the 5-nm Al_2O_3 shell functioning as the gate dielectrics, the metallic Co_2Si core functioning as the local top gate and the self-aligned platinum thin-film pads functioning as the source and drain electrodes (Fig. 1).

The Co_2Si nanowires were synthesized through a chemical vapour deposition process[27], with diameters typically in the range of 100–300 nm and lengths of around 10 μm (Fig. 2a). The composition of the Co_2Si was characterized by energy-dispersive X-ray spectroscopy (Supplementary Fig. 1). The Co_2Si–Al_2O_3 core–shell nanowires were grown through atomic layer deposition (ALD) of Al_2O_3 on the Co_2Si nanowires with controlled thickness. The relative dielectric constant of the deposited Al_2O_3 is determined to be ~7.5 on the basis of capacitance–voltage measurements using a planar metal/Al_2O_3/Si control structure. Transmission electron microscopy (TEM; Fig. 2b) shows a uniform coating of the amorphous Al_2O_3 surrounding the single-crystalline Co_2Si core. High-resolution TEM clearly shows the single crystalline Co_2Si core with an amorphous Al_2O_3 shell (Supplementary Fig. 2). Electrical measurements on a Co_2Si nanowire show linear current–voltage characteristics (Fig. 2c), with a 180-nm-diameter, 3-μm-long Co_2Si nanowire having a resistance close to 527 Ω and an estimated resistivity of 437 μΩ cm. Our measurements of over ten nanowires give a resistivity range of 200–500 μΩ cm, consistent with a previous report[27]. The low resistance of the Co_2Si nanowires is particularly important for them to function as effective gate electrodes for radio-frequency graphene transistors.

Figure 3a shows a SEM image of a self-aligned graphene transistor and an optical microscope image of the overall device layout (Fig. 3a, inset). The cross-sectional SEM image of a typical device shows that the self-aligned platinum thin-film source and drain electrodes are well separated by the nanowire gate and are precisely positioned next to the nanowire gate (Fig. 3b), demonstrating that the self-alignment process can be used to effectively integrate graphene with a nanowire gate and nearly perfectly positioned source and drain electrodes.

Before the formation of the self-aligned platinum source and drain electrodes, we measured the transfer characteristics: drain–source current (I_{ds}) versus the top-gate voltage (V_{TG}) applied by the local nanowire gate. The I_{ds}–V_{TG} plot shows that the graphene transistor can be modulated by the local nanowire gate, switching from the hole branch to the electron branch within a −1 V to +3 V range (Fig. 3c). This demonstrates that the Co_2Si–Al_2O_3 core–shell nanowire can indeed function as an effective local gate for the graphene transistors. However, the gate modulation is less than 10%, which is smaller than the typical values (around 50%) observed in graphene transistors at room temperature (25 °C). This difference can be attributed to the large access resistance due to the relatively small size of the gated area in comparison with the entire graphene channel.

The formation of the self-aligned source and drain electrodes allows precise positioning of the source–drain edges with the gate edges, and thus substantially reduces the access resistance and improves the performance of the graphene transistor. Before characterizing the transistor

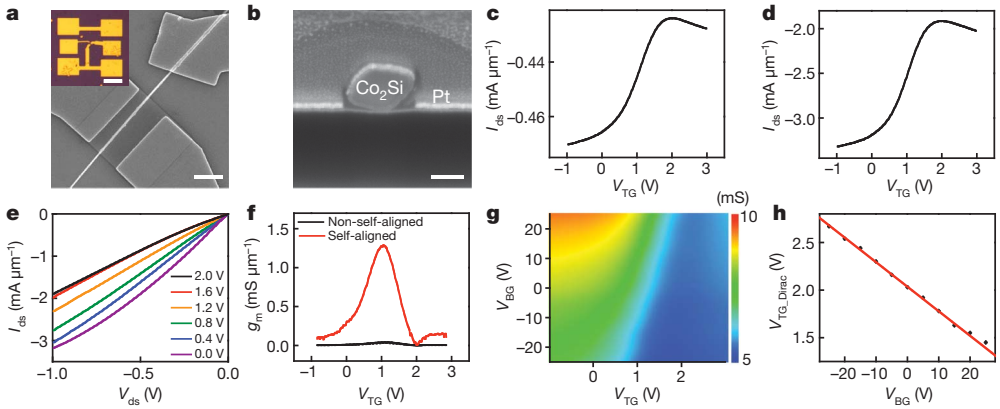

Figure 3 | Room-temperature electrical characteristics of the graphene transistors with a self-aligned nanowire gate. **a**, SEM images of a graphene transistor with a self-aligned nanowire gate. Scale bar, 1 μm. Inset, an optical microscope image of the overall device layout; scale bar, 50 μm. **b**, Cross-sectional SEM image of a typical device showing that the self-aligned platinum thin-film source and drain electrodes are well separated by the nanowire gate and precisely positioned next to the nanowire gate. The graphene below the nanowire gate is not clearly visible. Scale bar, 50 nm. **c**, **d**, I_{ds}–V_{TG} transfer characteristics at $V_{ds} = -1$ V before (**c**) and after (**d**) the deposition of the self-aligned platinum source and drain electrodes. **e**, I_{ds}–V_{ds} output characteristics at various gate voltages (V_{TG} = 0.0, 0.4, 0.8, 1.2, 1.6 and 2.0 V) for the self-aligned device. **f**, Transconductance, $g_m = |dI_{ds}/dV_g|$, at $V_{ds} = -1$ V as a function of V_{TG} before (black) and after (red) the deposition of the self-aligned platinum source and drain electrodes, highlighting how the self-alignment process increases the peak transconductance by a factor of >60. **g**, Two-dimensional plot of the device conductance for varying V_{BG} and V_{TG} biases for the self-aligned device. **h**, The top-gate Dirac point V_{TG_Dirac} at different V_{BG} biases, from which we can derive $C_{TG}/C_{BG} \approx 38$.

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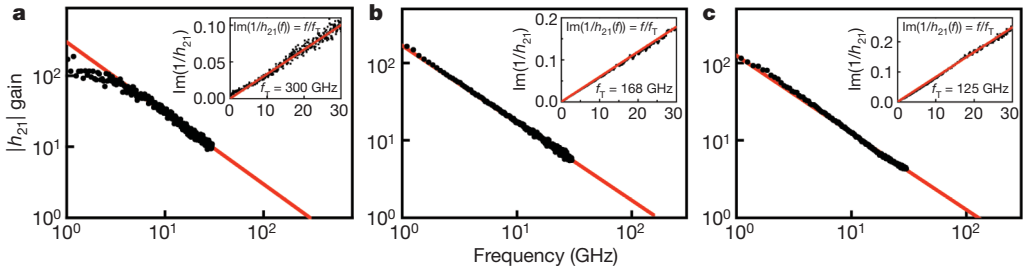

Figure 4 | Measured small-signal current gain $|h_{21}|$ as a function of frequency f at $V_{ds} = -1$ V. **a**, Gate length, 144 nm; $V_{TG} = 1$ V; **b**, Gate length, 182 nm; $V_{TG} = 0.3$ V; **c**, Gate length, 210 nm; $V_{TG} = 1.1$ V. The different V_{TG} values used are the peak transconductance points for each device. The insets show the extraction of f_T by Gummel's method.

properties of the self-aligned devices, we first tested the gate leakage across the Co_2Si–Al_2O_3–graphene gate stack. The gate tunnelling leakage current (I_{gs}) from the Co_2Si–Al_2O_3 core–shell nanowire to the underlying graphene is negligible within the gate voltage range of ± 3 V (Supplementary Fig. 3). This measurement demonstrates that the 5-nm Al_2O_3 dielectrics can function as an effective gate insulator for top-gated graphene transistors and afford the high gate capacitance that is critical to high transconductance.

Importantly, the I_{ds}–V_{TG} transfer curve measured for a self-aligned device shows a current modulation of about 42% (Fig. 3d), which is comparable to the typical values observed in long-channel graphene transistors and suggests that the access resistance in this ultrashort-channel device is greatly reduced through the self-alignment process. The hysteresis of I_{ds}–V_{TG} is about 0.02 V under ambient conditions (Supplementary Fig. 4), demonstrating the relatively clean nature of the graphene–dielectric interface. Figure 3e shows the I_{ds}–V_{ds} output characteristics at various gate voltages. The device can deliver a maximum scaled on-current of 3.32 mA μm^{-1} at $V_{ds} = -1$ V and $V_{TG} = -1$ V (Fig. 3d). The transconductance, $g_m = |dI_{ds}/dV_g|$, can be extracted from the I_{ds}–V_{TG} curve (Fig. 3f). A peak scaled transconductance of 0.02 mS μm^{-1} is obtained at $V_{ds} = -1$ V for the device before the deposition of the self-aligned source and drain electrodes. Significantly, with the self-aligned source and drain electrodes, the peak scaled transconductance at $V_{ds} = -1$ V reaches 1.27 mS μm^{-1}, a >60-fold improvement over the non-self-aligned device. This study shows that the self-alignment process is critical to ensure high transistor performance in the short-channel devices. To our knowledge, the scaled on-current and transconductance values obtained here are the highest values reported so far in bulk graphene transistors[11–13,15–17,28]. Higher transconductance was only observed previously in graphene nanoribbon transistors with much larger gate capacitance[25].

To characterize the gate capacitance, we measured the device conductance as a function of both V_{TG} and back-gate bias (V_{BG}) (Fig. 3g). From these measurements, we can obtain Dirac-point shifts in the top-gated configuration as a function of the applied V_{BG} (Fig. 3h), which gives the ratio between the top-gate and back-gate capacitances, $C_{TG}/C_{BG} \approx 38$. For a back-gate capacitance of $C_{BG} = 11.5$ nF cm^{-2}, the top-gate capacitance is estimated to be $C_{TG} = 437$ nF cm^{-2} (refs 11 and 24), which is consistent with the result, $C_{TG} \approx 394$ nF cm^{-2}, obtained from finite-element calculations (Supplementary Fig. 5).

The above discussions show that our self-aligned nanowire gate can be used to fabricate graphene transistors with unprecedented d.c. performance. An important benchmark of the transistor radio-frequency performance is the cut-off (transit) frequency, f_T. To assess the radio-frequency characteristics of our self-aligned transistors, on-chip microwave measurements were carried out in the range of 50 MHz–30 GHz using an Agilent 8722ES network analyser. Owing to the extremely small dimensions of our devices, the gate capacitance of our device is typically about two orders of magnitude smaller than the parasitic pad capacitance. To accurately determine the intrinsic f_T values requires careful de-embedding procedures (Methods)[13,14,17].

Figure 4a shows the $|h_{21}|$ current gain derived from the measured scattering parameters at $V_{TG} = 1$ V and $V_{ds} = -1$ V. It has the typical $1/f$ frequency dependence expected for an ideal field-effect transistor, yielding an f_T of 300 GHz. We also verified f_T data using Gummel's approach[29], in which the extracted f_T is identical to the aforementioned value (Fig. 4a, inset). This extracted f_T value is also consistent with the projected value (323 GHz) calculated using the well-known relation $f_T = g_m/(2\pi C_g)$ established for conventional field-effect transistors[30]. The speed of our self-aligned graphene device is the highest in all graphene devices reported so far[12–14,16–18]. Furthermore, it is about twice as fast as the best silicon MOSFETs of comparable sizes (for example about 150 GHz for a 150-nm silicon MOSFET) and is similar in speed to the best InP high-electron-mobility transistors and GaAs metamorphic high-electron-mobility transistors with similar channel lengths[10]. Figure 4b, c further shows the results obtained from another two self-aligned graphene transistors with 182-nm and 210-nm nanowire gates, for which $f_T = 168$ and 125 GHz, respectively.

It should be noted that the high intrinsic f_T values reported here are obtained after careful de-embedding procedures using the exact contact pad layout. Without de-embedding procedures, the extrinsic f_T values (2.4, 1.9 and 1.6 GHz) for the three devices described above are substantially lower (Supplementary Fig. 6), owing largely to the large ratio between the parasitic and gate capacitances. The large intrinsic f_T/extrinsic f_T ratios (125, 88 and 78) call for further scrutiny and validation of our de-embedding procedures. To this end, we have carefully analysed the second device to extract all device component values based on the equivalent circuit and scattering-parameter measurements (Supplementary Fig. 7). The device component values (including parasitic capacitance, gate capacitance, transconductance and so on) derived from the radio-frequency measurements are consistent with those obtained from the d.c. measurements or electrostatic simulations (Supplementary Tables 1 and 2). In particular, this analysis confirms that the difference between the intrinsic and the extrinsic f_T can be primarily attributed to the large ratio between the parasitic pad capacitance and the gate capacitance. By redesigning the device layout to reduce the parasitic capacitance, we can significantly reduce the parasitic capacitance/gate capacitance ratio and, hence, the intrinsic f_T/extrinsic f_T ratio (Supplementary Fig. 8). These studies unambiguously validate our de-embedding procedures.

The unprecedented transistor performance achieved in the self-aligned devices should open exciting opportunities in high-speed, high-frequency electronics. With further optimization of large-area graphene growth, nanowire assembly or a soft lithography process to precisely control the dimension and location of the self-aligned gate, large arrays of self-aligned high-speed graphene transistors or circuits could be produced.

METHODS SUMMARY

We synthesized the nanowires and fabricated the transistors as described in the main text. The d.c. electrical transport studies were conducted with a probe station at room temperature (25 °C) under ambient conditions with a computer-controlled analogue-to-digital converter. The on-chip microwave measurements were carried out in the 50 MHz–30 GHz range using an Agilent 8722ES network analyser. The measured scattering parameters were de-embedded using specific 'short' and 'open' structures with identical layouts, excluding the

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graphene channel, to remove the effects of the parasitic capacitance, resistance and inductance associated with the pads and connections. The 'through' calibration was done with the exact pad layout with the gate shorted to the drain, and the 'load' calibration was done with the standard calibration pad layout.

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Supplementary Information is linked to the online version of the paper at www.nature.com/nature.

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Author Contributions X.D conceived the research. X.D. and L.L. designed the experiments. L.L. performed all the experiments (including material synthesis, device fabrication, and d.c. and radio-frequency characterization) and data analysis. Y.-C.L. contributed to material synthesis, material and device structure characterization, and radio-frequency analysis. M.B. contributed to radio-frequency characterization and analysis. R.C. and Y.L. contributed to d.c. and radio-frequency analysis. J.B. contributed to device fabrication. Y.Q. contributed to material synthesis. X.D. and L.L. co-wrote the paper. All authors discussed the results and commented on the manuscript.

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