Low Write-Energy Magnetic Tunnel Junctions for High-Speed Spin-Transfer-Torque MRAM

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***Abstract*—This letter presents energy-efficient MgO based magnetic tunnel junction (MTJ) bits for high-speed spin transfer torque magnetoresistive random access memory (STT-MRAM). We present experimental data illustrating the effect of device shape, area, and tunnel-barrier thickness of the MTJ on its switching voltage, thermal stability, and energy per write operation in the nanosecond switching regime. Finite-temperature micromagnetic simulations show that the write energy changes with operating temperature. The temperature sensitivity increases with increasing write pulsewidth and decreasing write voltage. We demonstrate STT-MRAM cells with switching energies of < 1 pJ for write times of 1–5 ns.**

***Index Terms*—Magnetic tunnel junctions (MTJs), magnetoresistive random access memory (MRAM), nonvolatile memory, spin transfer torque (STT).**

I. Introduction

MAGNETORESISTIVE random access memory (MRAM) utilizing the spin transfer torque (STT) effect has become a focus of research and development in recent years due to its combination of high speed, high density, nonvolatility, scalability, and endurance, which makes it a promising candidate for replacing several competing memory technologies for both embedded and stand-alone applications [1]–[8]. Typically, MgO-based magnetic tunnel junction (MTJ) structures are used as the memory element in STT-MRAM circuits due to their fairly low switching-current density (compared with metallic spin valves) as well as large resistance and tunneling magnetoresistance (TMR) ratio compatible with read and write in integrated CMOS technology [1]–[5].

In MTJ cells with in-plane magnetization used for STT-MRAM, thermal stability is determined by the volume of the magnetic free layer and its saturation magnetization, as well as its magnetic anisotropy field and is, thus, a function of the bit area, film thickness, and aspect ratio [3], [7]–[9]. For optimal bit operation, one must prevent false-switching events induced by thermal activation while minimizing the energy dissipation during current-induced switching of the magnetic bits (i.e., the write energy). This is a challenge in high-speed memory applications, with write times in the nanosecond range, where the required switching current densities are high compared with those in quasi-static or long-pulse switching. An understanding of the tradeoffs between thermal stability and write energy, including the effects of device size, shape, and temperature, is thus critical for optimizing the performance of STT-MRAM cells.

In this letter, we report thermally stable MTJ cells with ultralow write energies for application in high-speed STT-MRAM. The devices exhibit write energies as small as 0.3 to 0.8 pJ with write times of 1–5 ns. The effects of MgO film thickness, memory bit size, and shape on these performance parameters are experimentally investigated. Finite-temperature micromagnetic simulation results reveal a reduction in the write energy with increasing operation temperature. The temperature sensitivity of the switching energy is increased for longer write pulselengths, where thermal activation effects play a more prominent role.

II. Experiment

MTJs with a composition of (bottom electrode)/PtMn (15 nm)/CoFe (2.5 nm)/Ru (0.85 nm)/CoFeB (2.4 nm)/MgO/CoFeB (1.8 nm)/(top electrode) were sputter deposited using a Singulus TIMARIS PVD system, followed by annealing under a field of 1 T at 300 °C for 2 h. The MgO film was deposited using an RF magnetron sputter process, whereas all other layers were deposited by dc magnetron sputtering. The MTJ films were then patterned into elliptical nanopillars with a range of sizes and aspect ratios. The MgO layer thickness was varied across the wafer to study the effect of tunnel-barrier thickness on the device characteristics.

The measured TMR ratio and resistance–area (RA) product of the nanopillars as a function of MgO thickness, determined from R–H loops along the easy axis (pillar length) of the MTJ cells, are shown in Fig. 1. These are in agreement with

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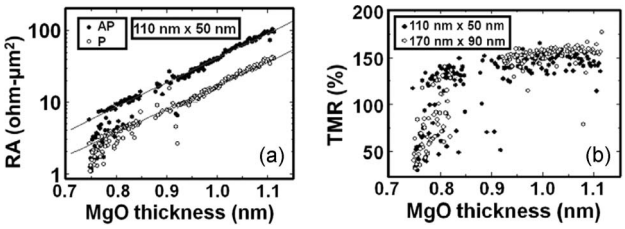

Fig. 1. (Left) RA product and (right) TMR ratio of MTJs as a function of MgO barrier thickness.

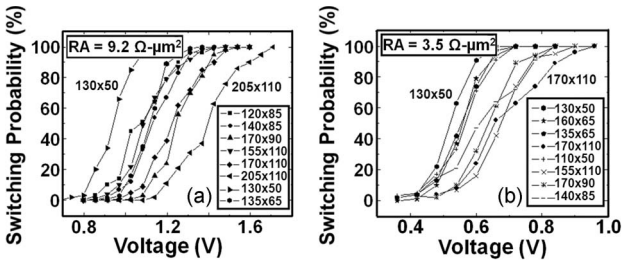

Fig. 2. Probability of current-induced switching from antiparallel (high-resistance) to parallel (low-resistance) states in a series of MTJs for two values of the RA product. With free- and fixed-layer magnetizations being in plane and collinear, the free-layer switching is subject to thermal activation and, thus, a probabilistic function of the applied pulse voltage. While the switching voltage increases for higher RA products, it also depends on device area and aspect ratio. Moreover, note that the write voltage does not scale with resistance, indicating an increase in switching-current density with reducing MgO barrier thickness. Device dimensions are given in nanometers.

current-in-plane tunneling (CIPT) measurement results on the unpatterned wafer. Typical coercivities were in the range of 50–100 Oe. The junction resistance for both parallel and antiparallel magnetization orientations increases with barrier thickness as expected, while the TMR ratio remains almost constant over a wide MgO thickness range. Both RA and TMR exhibit a sharp drop for MgO thicknesses smaller than ∼0.8 nm as a result of increased pinhole density in the thin barriers. The measured RA product does not show a significant dependence on the junction area, indicating the absence of sidewall shorts. For reliable device operation, one would like to choose the MgO thickness in a range to obtain a high TMR ratio while ensuring a low RA to maintain small write voltages and low write energies, as discussed subsequently. In the following, we present and compare results for devices with RA values of 3.5 and 9.2 $\Omega \cdot \mu\text{m}^2$ in the parallel state.

Current-induced switching measurements were performed using 5 ns voltage pulses applied to the devices using a probe station in a one-port ground–signal–ground configuration. Repeated switching measurements were performed to obtain the switching probability as a function of write voltage across the junction (see Fig. 2). The write energy was then obtained from $E_w^{\text{AP}\to P} = V_m^2 \tau / R_{\text{AP}}$. Here, V_m is the mean write voltage at the device, corresponding to a 50% probability of switching, and is related to the incident pulse voltage V_p by $V_m = 2V_p R_{\text{AP}}/(R_{\text{AP}} + Z_0)$ due to the mismatch between the high MTJ resistance and the $Z_0 = 50\ \Omega$ system impedance [10]. The pulsewidth is $\tau = 5$ ns, and R_{AP} is the MTJ resistance in antiparallel state. The write energy for switching from parallel to antiparallel states $E_w^{P\to\text{AP}}$ can be similarly defined using the parallel-state resistance R_P and the corresponding probability

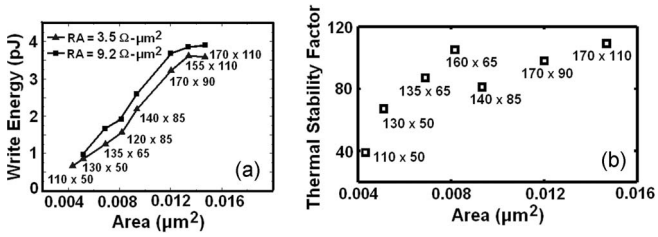

Fig. 3. (a) Switching energy of MTJ cells with different sizes for two values of the RA product. MTJ dimensions are given in nanometers. While the reduced switching voltage in devices with low RA results in a reduction of the write energy, the improvement is limited due to the simultaneous increase in the switching-current density with reduced MgO thickness. (b) Thermal stability of STT-MRAM cells. Note the increase with both size and aspect ratio. The thermal stability is determined by the free-layer properties and does not exhibit a significant dependence on the MgO barrier thickness. Note that, while other thermal stability characterization approaches (e.g., based on pulsewidth dependence of the switching voltage or sweep-rate dependence of the coercivity) might result in smaller values for the thermal stability factor, the trends (i.e., size and shape dependence) shown in this figure are independent of the characterization approach.

curve and is, in general, different from $E_w^{\text{AP}\to P}$ due to the differences in the switching-current and resistance in the two cases [4]–[6]. Note that, under typical operating conditions, significantly lower write-error rates are required, leading to higher switching-energy values. In the following, we only refer to write energies obtained for switching from antiparallel to parallel states, although the conclusions remain valid for the reverse direction as well. Switching energies for a number of pillar dimensions and two RA products are shown in Fig. 3(a).

The thermal stability factor of the MTJs can be defined as $\Delta = E_V/k_BT$. Here, E_V denotes the energy barrier between the free-layer states, and k_B and T correspond to the Boltzmann constant and temperature, respectively [7]–[9]. The energy barrier is given by $E_V = M_s H_k V/2$, where M_s is the free-layer saturation magnetization, V is its volume, and H_k is the magnetic anisotropy field. The latter was determined from R–H curves measured along the pillar hard axis as well as from spin-torque ferromagnetic resonance measurements. It contains both the magnetocrystalline anisotropy field induced during deposition and annealing and the shape-induced anisotropy which gives rise to an easy axis along the magnetic pillar and is the main mechanism responsible for thermal stability in our devices. Values for Δ measured for a number of different pillar dimensions are shown in Fig. 3(b).

Device endurance was characterized through accelerated time-dependent dielectric-breakdown measurements using 5 ns pulses with amplitudes of > 0.9 V and subsequent extrapolation to operating voltages. Endurance of $> 10^{16}$ write cycles was estimated in this manner for MTJ cells with RA $= 3.5\ \Omega \cdot \mu\text{m}^2$ (see Fig. 4).

III. Discussion

While the write energy exhibits a general increase for increasing device areas, as shown in Fig. 3(a), its value also depends on the MgO barrier thickness (i.e., RA product). Devices with thicker tunnel barriers exhibit larger write energies, mainly due to the larger voltages required to switch them (see voltages in Fig. 2). As a result, to optimize the magnetic bit for

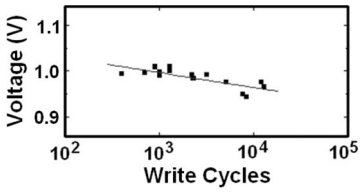

Fig. 4. Accelerated dielectric-breakdown measurements using 5 ns pulses at voltages > 0.9 V were used for endurance characterization. The estimated endurance based on extrapolation to normal operating voltage is $> 10^{16}$ write cycles for devices with RA $= 3.5\ \Omega \cdot \mu\text{m}^2$.

low write energy, the tunnel-barrier thickness should be chosen to be small while maintaining a high TMR ratio. This is also necessary in order to keep the write voltages small for low-power CMOS integration. For a given RA product, Fig. 2 shows that devices with larger areas exhibit a higher switching voltage despite their lower resistance. This indicates an increase in the switching-current density with increasing device area, presumably due to excitation of nonuniform dynamic magnetization modes during switching in the larger devices.

Thermal stability factors for a number of magnetic-bit geometries are shown in Fig. 3(b). Note that while Δ increases with the area (hence volume) of the free layer, a significant dependence on pillar aspect ratio is also evident, which can be attributed to increased shape anisotropy for pillars with larger aspect ratios. (Compare, e.g., thermal stabilities for 160 nm $\times$ 65 nm and 140 nm $\times$ 85 nm devices). For 130 nm $\times$ 50 nm devices with RA $= 3.5\ \Omega \cdot \mu\text{m}^2$ and $\Delta > 60$, write energies as small as $\sim$0.8 pJ were observed at 5 ns write time. Reducing the pulsewidth to 1 ns further reduced the write energy to $\sim$0.3 pJ while increasing the write voltage from 0.6 to 0.9 V. A standard deviation of $\sim$20% was observed for both write energy and thermal stability in these devices.

When integrated with CMOS, the operating temperature of STT-MRAM can be significantly higher than room temperature, affecting thermal stability. Moreover, within the thermally activated switching regime, increased temperature can facilitate easier switching and reduce the write energy [8], [9]. Hence, optimization for a given write energy and stability performance depends on the targeted operating temperature. Micromagnetic simulations were used to investigate the temperature dependence of write energy in the MTJ cells. The micromagnetic solver [11] included a stochastic Langevin term in the Landau–Lifshitz–Gilbert equation to account for thermal activation effects. The device consisted of a 110 nm $\times$ 50 nm pillar with RA $= 3.5\ \Omega \cdot \mu\text{m}^2$ and TMR $= 110\%$, for which we experimentally obtained a mean write voltage of 0.57 V at 5 ns write time (see Fig. 2). Write voltages of 0.4 and 0.5 V were considered in the simulations, and the write energy for a given voltage was calculated using the mean switching time τ_m, obtained from 100 repeated simulation runs. For the case of 0.5 V write pulse amplitude, we observed a reduction of τ_m from 12.6 to 11.8 ns when the temperature was increased from 300 to 380 K, corresponding to a slight reduction of write energy from 3.9 to 3.6 pJ. Using 0.4 V pulses, however, increased the switching times considerably and enhanced the effect of temperature on the write energy. In this case, we observed a reduction of τ_m from 46.4 to 31.2 ns over the same temperature range, corresponding to reduction of write energy from 9.2 to 6.2 pJ. Smaller write voltages (i.e., longer pulsewidths) thus result in a stronger dependence of the write energy on temperature, indicating the more pronounced role of thermal activation in the switching process.

IV. Conclusion

MTJs with write energies < 1 pJ and write times < 5 ns have been experimentally demonstrated. The low write energy was realized using a combination of low RA product (while maintaining TMR $> 100\%$) and adjustment of free-layer volume and aspect ratio to maintain thermal stability. The dependence of write energy on MgO thickness was studied experimentally. Micromagnetic simulations revealed a dependence of switching properties on operation temperature, with the write energy for a given device showing stronger temperature sensitivity for smaller write voltages.

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